A 6-bit Low-Power High-Speed Flash ADC using 180 nm CMOS process

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ABSTRACT

In this paper we present a design of Flash-ADC that can achieve high performance and low power consumption. By using the Double Sampling Rate technique and a new comparator topology with low kick-back noise, this design can achieve high sampling rate while still consuming low power. The design is implemented in a 0.18 μm CMOS process. The simulation results show that this design can work at 400 MSps and power consumption is only 16.24 mW. The DNL and INL are 0.15 LSB and 0.6 LSB, respectively.

Key words: *Flash ADC, comparator, double sampling sample-and-hold, glitch effect*

INTRODUCTION

With the development of digital signal processing (DSP) techniques in different domains, such as wireless communications, medical electronics, video and measurement instrumentations, many applications need an analog-to-digital (ADC) chip. So ADC plays an important role as the bridge between the analog world and digital world. The basic function of an ADC is to convert analog signal to digital signal. In the field of high speed ADC, Flash ADC is the best candidate. To achieve high sampling rate, the parallel structure is employed in Flash ADC. The input analog signal will be compared to the referent voltage in parallel.

The penalty for the parallel operation in Flash ADC is power consumption and chip area. *N*-bit Flash ADC needs 2^{N-1} comparators which consume a lot of power and need a large chip area. Therefore, this is an issue that we must trade off, especially when ADC is a part of total LSI chip and power is supplied by a battery as well [1]. There are several ways to reduce the power at the same speed and accuracy. Although technology scaling can lower the power, device mismatch will be increased thus posing greater design challenges for obtaining the required resolution. For a given CMOS technology, alternative circuit techniques, such as time interleaving, requires multiple accurately-speed clocks, and furthermore mismatches in interleaved comparators can cause distortion and spurious tones [3]. Also in a folding architecture, high folding factor results in reduced power consumption, but on the contrary, it lowers the maximum input signal frequency of the A/D converter [4]. In [6], comparators with built-in reference levels have been used to estimate the comparator thresholds in order to remove the

static power of the conventional reference ladder. However, the ADC performance is degraded due to the device mismatches. A power reduction technique is presented in [11] based on the principle of turning off the preamplifier of the comparators after the time when output voltages have been decided using an XOR gate. The drawback is complexity and large area chip.

In this paper we describe the concept, design and experimental results of a 6-bit flash-ADC, optimized for low power while maintaining comparable power consumption. By employed a new low kick-back noise comparator, double sampling sample-and-hold and the glitch cancelation scheme, the power of the proposed Flash ADC is reduced to less than 20 mW while 400 MSps sampling rate can be achieved.

METHODS

Proposed architecture

The proposed Flash ADC architecture is shown in Fig. 1 and the specification is in Table 1. A flash converter consists of 2^N resistor connected in serial to create 2^{N-1} referent voltages where N is the number of output bits. The input analog signal will be compared to these referent voltages at the same time. Flash ADC needs 2^N comparators. The input signal is converted in only one cycle. After the sampling clock becomes active, a part of the comparator circuits has an input signal lower than the local ladder voltages will generate a logical "zero", while the other comparators will generate a logical "one". The digital code on the outputs of the comparators is called a "thermometer code". A digital encoder circuit converts the thermometer code to an N-bits output format. In general, ROM encoder is employed because of its simplicity and low cost. The draw-back of ROM encoder is sensitive with the bubble error. When bubble errors happen, two or more word lines are opened at the same time. It causes the invalid output codes. To overcome this issue, a bubble circuitry is needed. The roles of the bubble circuitry are to convert the "thermometer code" to "one-hot code", detect and correct errors. It guarantees only one word line is opened at the time.

When the comparators are in evaluating state, the input signal must be constant. So a sample and hold circuitry is needed. After the output code is valid, it will capture by N latch circuitries instead of 2^{N-1} as the conventional Flash ADC. It helps save total chip area and increase produce yield as well.

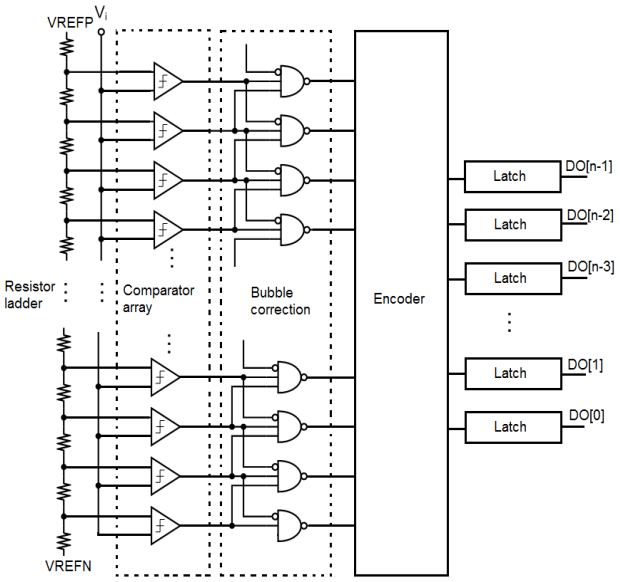

Fig. 1. The proposed Flash ADC architecture

Table 1. ADC specification

Character	Value
Process	180 nm
Sampling rate	400 Msps
Analog input signal	0 V ÷ 1 V
Voltage supply	1.8 V ± 10 %
Resolution	6 bit
Power	< 20 mW

New low kick-back noise comparator

In any ADC, comparators are the most critical components because their input offset voltage, delay and input range directly influence the resolution and speed of the ADC. Furthermore, the noise generated within a comparator itself plays an important role in its overall performance at high frequency [1]. In order to achieve the high speed and low power consumption, the dynamic comparator is employed. The draw-back of dynamic comparators is that they need a clock signal and kick-back noise. The conventional dynamic comparator is as Fig. 2. Because of the intrinsic parasitic inside MOSFET transistors, there are capacitances connected drain/source terminal to gate terminal. So the clock signal can create a kick-back pulse to input analog signal and the reference voltages as denoted in Fig. 3. This effect is called kick-back noise. The kick-back noise becomes bigger when there are a lot of comparators are connected in parallel. This limits the performance and resolution of the Flash ADC.

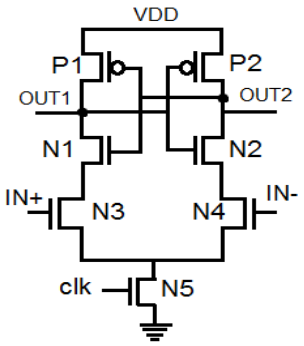

Fig. 2. The conventional dynamic comparator

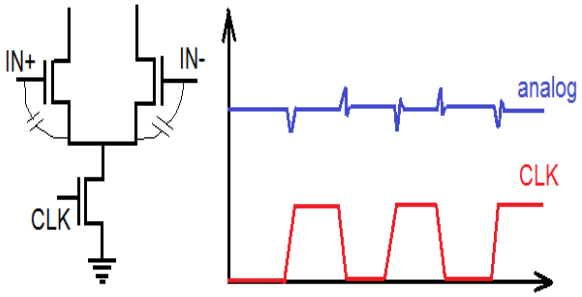

Fig. 3. Kick-back noise

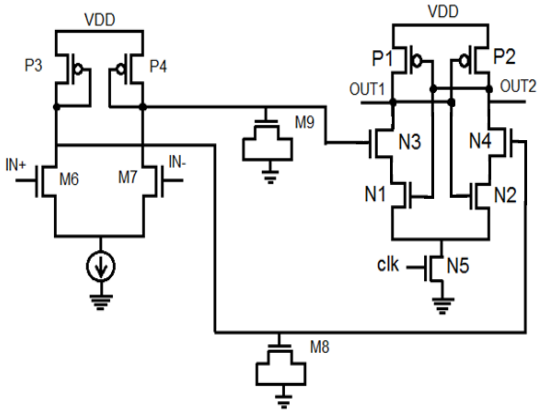

Fig. 4. The proposed comparator with very low kick-back noise

Table 2. Kick-back noise comparison

Comparator topology	Kick-back voltage (63x1 array)	%
Conventional	22mV	
With pre-amplifier	5.6mV	-74.4
With pre-amplifier and MOS capacitors	2.1mV	-90.45

Double sampling Sample-and-Hold circuitry

A sample-and-hold circuitry is a crucial part in a high-speed A/D converter. In general, the conversion consists of two phase: sample and evaluate phase. In the sample phase, the input will charge the capacitor named C_{hold}. In the evaluation phase, the signal is hold at constant value by C_{hold} and evaluated by the comparators. With this scheme, the comparators will suspend at sample phase and cause waste of time. A double sampling sample-and-hold can be used to resolve this disadvantage. A double sampling sample-and-hold is described as Fig. 5.

The capacitors of two parallel channels working on opposite clock phases and share the same amplifier. When Φ1 is high, switch S1/S4 are closed and S2/S3 are opened. As the result, C1 and C2 are working in sampling mode and hold mode, respectively. When Φ2 is high, the operation of C1 and C2 are inverted. With this architecture, the input signal is always available for comparator and the comparator can operation at both phases. Thus, the sampling rate is twice times increased while maintaining comparable power consumption.

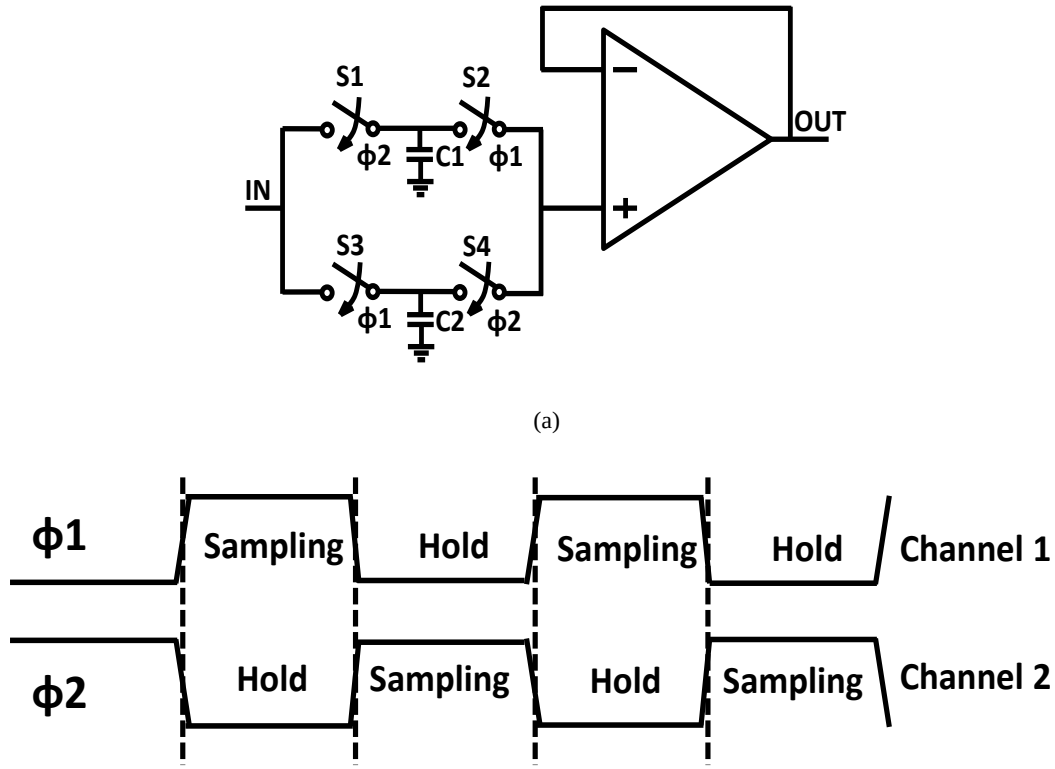

Fig. 5. Double sampling Sample-and-Hold scheme. (a) Circuit symbol. (b) Waveform of operation

Glitch cancelation scheme

Glitch is an important issue in high speed circuit. Glitch pulses cause power increasing and invalid output codes. In this design, we propose a scheme to control the operation of all blocks with exactly timing that minimize the effect of glitch. The control unit is describe as Fig. 6 and its timing diagram is shown on Fig. 7

Firstly, the input signal is sampled by the rising edge of φ1 while ROM encoder is pre-charged in short period of time so that all bit lines are pulled up to VDD by the falling edge of Clk1. After input signal is stable, comparators are enabled at the rising edge of Clk2. The comparators will evaluate the input signal and the referent voltage. The bubble circuitry converts the thermometer code to one-hot code and then converted to *N* bit binary code by ROM encode. When code is valid, the latches will be opened and capture data at the rising edge of Clk3. With this scheme we can control the operation of each block in harmony. Thus, we can reduce glitch effect and save power.

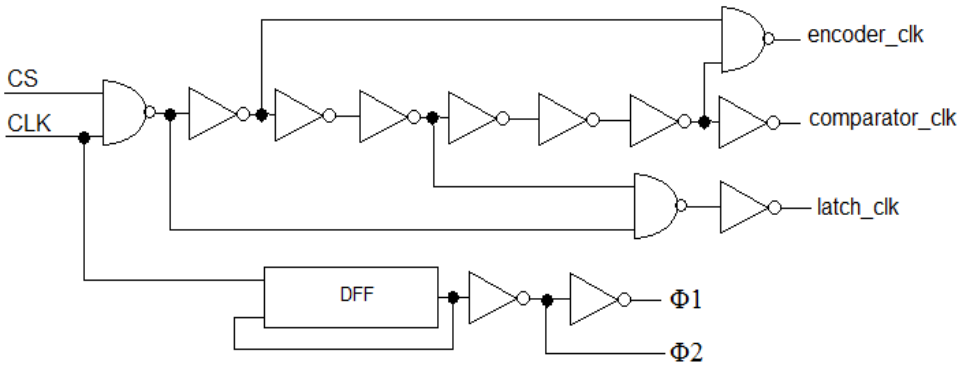

Fig. 6. Schematic of control unit

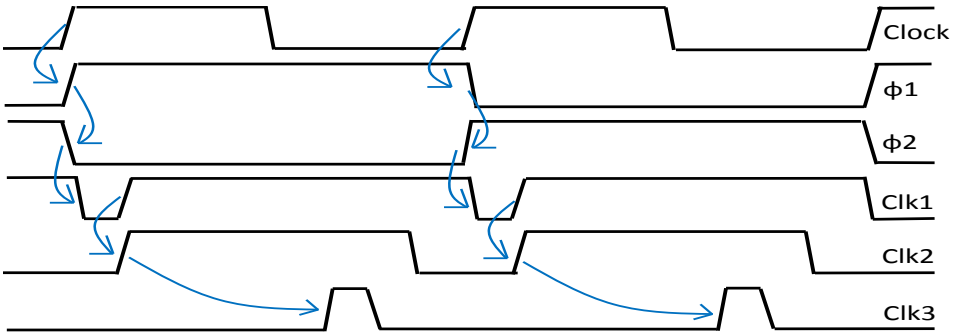

Fig. 7. Generated clock waveform

Table 3. Dynamic parameter versus input signal frequency

Fin	Fs	SNR	SINAD	SFDR	ENOB
5.4Mhz	400Mhz	36.72	35.39	43.30	5.6
8.5Mhz	400Mhz	35.83	33.58	38.54	5.3
10Mhz	400Mhz	35.22	32.69	37.27	5.2

RESULTS

The proposed ADC has been implemented by a 0.18 µm CMOS process and post-layout simulation results are carried out. The supply voltage is 1.8 V and the sampling rate is 400 Msps. The layout of chip is shown in Fig. 8 with total area is 0.15 mm^2. Total MOSFET devices are 3635. The DNL and INL shown in Fig. 9 are simulated with an input ramp signal sampled at maximum frequency. The peak DNL and INL are 0.15 LSB and 0.6 LSB, respectively.

Fig. 10 illustrates the output spectrum at 400 MSps and a 5.4 MHz input signal frequency. Table 3 describes the simulated spurious free dynamic range (SFDR), signal-to-noise ratio (SNR), SINAD and ENOB versus input signal frequency. Table 4 shows that this design can achieve many advantages in comparison to other studies. Compared to [1], [2] and [3], the proposed design has been saved the power up to 80.17% while the quality of ADC is kept higher. Compared to [3], DNL/INL value of the proposed ADC is larger. It is due to the nonlinear of pre-amplifier and sample-and-hold circuitry. The other reasons are that the ADC in [3] operates at lower frequency and uses a larger CMOS process. This means lower noise and process variation.

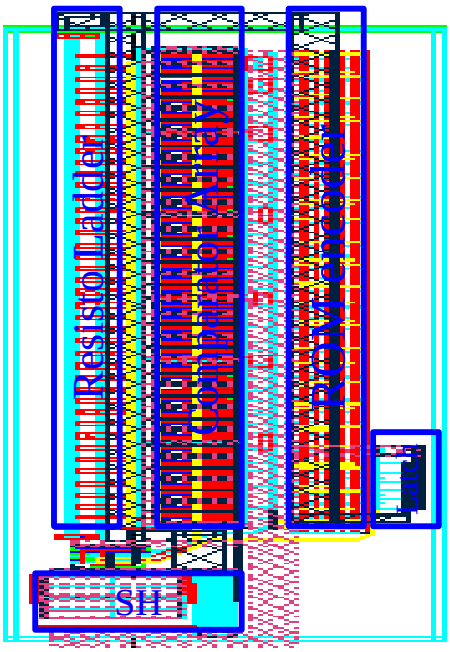

Fig. 8. Chip layout

Table 4. Comparison in power consumption with other publications

Specification	This work	(1)	(2)	(3)
CMOS tech (µm)	0.18	0.18	0.18	0.25
Sampling rate (MSps)	400	400	400	300
Resolution (bit)	6	4	6	6
Power supply (V)	1.8	1.8	1.8	2.5
DNL/INL (LSB)	0.15/0.7	0.4/1.1	< 0.5	0.1/0.4
Power (mW)	16.64	30	90	35

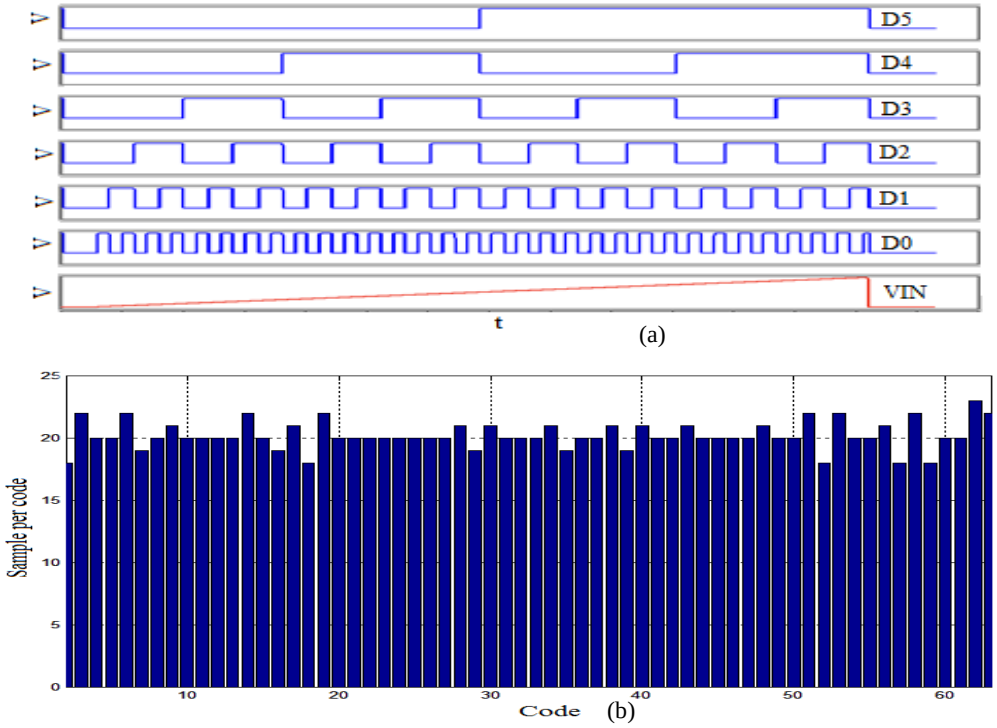

Fig. 9. DNL/INL measurement. (a) Wave form. (b) Number sample per code

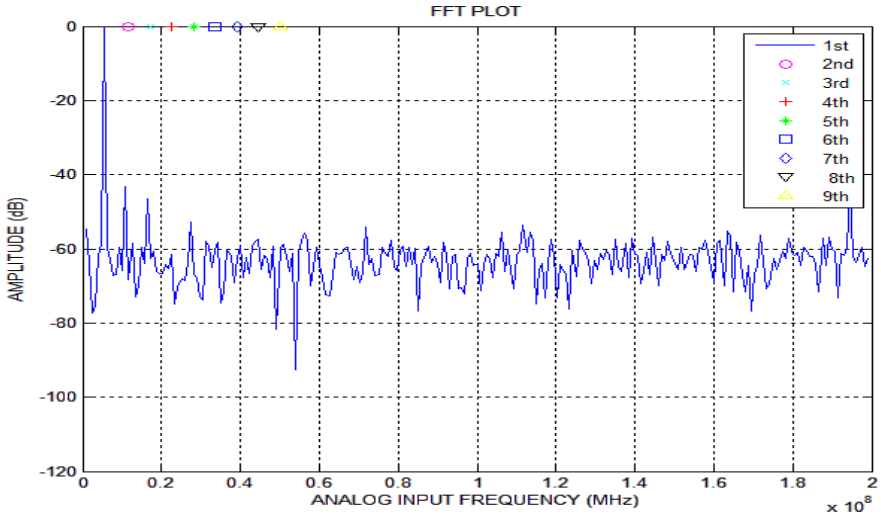

Fig. 10. Output spectrum of a 5.4 Mhz analog input signal at 400 MS/s

CONCLUSIONS

This paper has presented many techniques to reduce power consumption and chip area while still achieving high frequency requirement. The post layout simulation results show that the ADC works well at 400 MSps and consumes only 16.64 mW. Compared with some published papers, the proposed Flash ADC has many advantages in terms of power and area.

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Thiết kế bộ FLASH-ADC 6 BIT tốc độ cao, công suất thấp dùng công nghệ CMOS 180 nm

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TÓM TẮT

Bài báo này trình bày một thiết kế Flash-ADC có tốc độ cao và công suất thấp. Bằng cách áp dụng kỹ thuật Double sampling rate và kiến trúc mạch so sánh mới có nhiễu Kick-back thấp, thiết kế đạt được tốc độ chuyển đổi cao mà vẫn đạt được tiêu chí công suất thấp. Thiết kế được hiện thực dùng công nghệ CMOS 180nm. Kết quả mô phỏng cho thấy thiết kế hoạt động tốt ở tốc độ 400MSps, công suất tiêu thụ 16.64 mW, giá trị DNL và INL lần lượt là 0,15 LSB và 0,6 LSB.

Từ khóa: *Flash ADC, comparator, Double sampling sample-and-hold, glitch effect*

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