FPGA Implementation of Mimo E-SDM for future communications wireless networks

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ABSTRACT:

Multiple-input multiple-output (MIMO) systems applying the Eigenbeam-Space Division Multiplexing (E-SDM) technique can be considered as optimal MIMO systems because of providing the highest channel capacity and good communications reliability. In the systems, orthogonal transmission beams are formed between transmit and receive sides; and also optimal transmit input data are adaptively allocated. In addition, a simple detection can be used at receiver to totally eliminate sub-stream interference. Therefore, MIMO E-SDM systems have been considered as a good potential technology for future high speed data transmission networks. Although there have been a lot of technical papers evaluated the systems based on theory analyses and/or computer-based simulation, just few ones have been considered the MIMO E-SDM systems based on hardware design. The main contribution of this paper is to present our own design and implementation of 2x2 and 2x3 MIMO E-SDM systems on FPGA Altera Stratix DSP Development KIT using Verilog HDL, an important step before going to make integrated circuits. The bit-error rate performance the consumption for our design of these systems have shown that our design is successful.

Keywords: MIMO, E-SDM, ZF, FPGA, hardware design.

1. INTRODUCTION

Multiple-input multiple-out (MIMO) systems have been considered as a high speed data transmission technology. The channel capacity of the systems can increase significantly and is proportionally to the number of transmit (TX) and receive (RX) antennas without additional power and bandwidth compared with single-input single-out systems. The systems have been standardized to be used in modern networks such as IEEE 802.11, 3GPP Long Term Evolution, and WiMAX [1–3].

When channel state information (CSI) is not available at transmitter, spatial division multiplexing (SDM) technique is used for data transmission. In the technique, data resources, power level and modulation scheme, are allocated equally to all transmit sub-streams [4-6]. However, when CSI is available, an eigenbeam-space division multiplexing (E-SDM) is used [7-

9]. The MIMO E-SDM systems are also called singular value decomposition MIMO (SVD MIMO) systems [10] or MIMO eigenmode transmission systems [11].

In E-SDM techniques, an orthogonal beamforming is formed based on the eigenvectors obtained from eigenvalue decomposition using a MIMO channel matrix. To increase quality of the systems, the E-SDM technique has an innovation in transmitting. A new feature of this algorithm is the calculation of the bit error probability of each flow with many cases of demodulation. In the systems, a simple receive weight method can demultiplex received signals without inter-substream interference, and maximum channel capacity is obtained. These advantages make the MIMO E-SDM technology a promising candidate for future high-rate wireless applications.

There have been a lot of technical papers studied and evaluated about the MIMO E-SDM systems based on theory analyses and/or computer-based simulation [7-11]. However, just few ones have considered the systems based on hardware implementation [12,13].

The main contribution of the paper is to present our own detailed design and implementation of the MIMO E-SDM systems on FPGA Altera Stratix DSP Development KIT using Verilog HDL. We use HDL description in the whole system because we want an executable functional specification. Besides, the executable models can be tested and refined during implementation process. In addition, HDL description is the first step to build an implementation directly from a behavioral model in an automated process. Based on the design, we evaluate bit-error rate (BER) of the systems and also compare the consumption of FPGA elements for our design of the systems. A part of the paper has been presented in [14]. Moreover, we have also extended our study of single carrier MIMO E-SDM systems (presented in the paper) to multi-carrier MIMO E-SDM systems [15]. In the multi-carrier systems, Othogonal Frequency Division Multiplexing (OFDM) technique is used to improve frequency efficiency and eliminate inter-symbol interference.

The paper is organized as follows. In the next section, an overview of MIMO E-SDM systems is presented. In section III, we will show our design and hardware implementation of the MIMO E-SDM system. The results and discussion of our implementations are shown in section IV. Finally, conclusions are drawn in Section V.
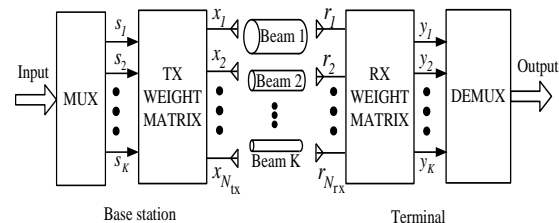
2. OVERVIEW OF MIMO E-SDM SYSTEMS

Fig. 1. Block diagram of MIMO E-SDM system

Consider a MIMO E-SDM system with N_{TX} antennas at TX and N_{RX} antennas at RX, as shown in Fig. 1. When MIMO CSI is available at the TX, orthogonal transmit eigenbeams can be formed between the TX and the RX. Eigenbeams are obtained from eigenvalue decomposition of

matrix $H^H H$, where H denotes as the MIMO channel matrix as following:

$$H = \begin{pmatrix} h_{11} & h_{12} & \cdots & h_{1N_{TX}} \\ h_{21} & h_{22} & \cdots & h_{2N_{TX}} \\ M & M & h_{ij} & M \\ h_{N_{RX}1} & h_{N_{RX}2} & \cdots & h_{N_{RX}N_{TX}} \end{pmatrix}, \quad (1)$$

At the TX side, an input stream is divided into K substreams (K ≤ min(N_{RX}, N_{TX})). Then, signals before transmission are driven by a transmit weight matrix W_{TX} to form orthogonal transmit beams and control power allocation. At the RX side, received signals are detected by a receive weight matrix W_{RX}. The optimal W_{TX} and W_{RX} are determined according to [7, 8] as

$$W_{TX} = U\sqrt{P}, \quad (2)$$

$$W_{RX} = U^H H^H, \quad (3)$$

where U is obtained by the eigenvalue decomposition as

$$H^H H = U\Lambda U^H, \quad (4)$$

$$\Lambda = diag(\lambda_1, \lambda_2, ..., \lambda_K), \quad (5)$$

where $\lambda_1 \geq \lambda_2 \geq ... \geq \lambda_K > 0$ are positive eigenvalues of $H^H H$. The columns of U are the eigenvectors corresponding to those positive eigenvalues, and $\sqrt{P} = diag(\sqrt{P_1}, \sqrt{P_2}, ..., \sqrt{P_K})$ is the transmit power matrix.

The detected signals in an ideal E-SDM system are given by

$$y(t) = \Lambda\sqrt{P}s(t) + W_{RX} n(t), \quad (6)$$

where s(t) is a transmit signal vector and n(t) is AWGN noise at RX. The result from (6) shows that the ESDM technique transforms the MIMO channel into K orthogonal subchannels. The signal-to-noise power ratio (SNR) of the kth substream is given by $\lambda_k P_k P_s / \sigma^2$. This indicates that the quality of each substream is different. Therefore, the channel capacity and BER performance can be improved by adaptively assigning the data rate and transmitting power [7, 8].

3. DESIGN AND IMPLEMENTATION OF MIMO E-SDM SYSTEMS

The block diagram of our design and implementation of a 2x2 MIMO E-SDM system on FPGA hardware is shown in Fig. 2. For the case of 2x3 system, it will be designed and implemented similarly.
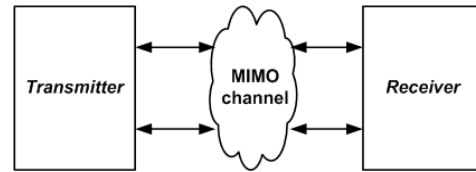

Fig. 2. Design of a 2x2 MIMO E-SDM system

3.1. Transmitter side

In the TX side, we need to estimate CSI matrix H fedback from the RX, and then determine the eigenvalue and eigenvector. Based on these values, transmit data resources and power allocation are calculated. The TX also consists of other modules such as data generator, digital modulations, adding sending choice, adding training symbols, normalizing and transmitting, as shown in Fig. 3.
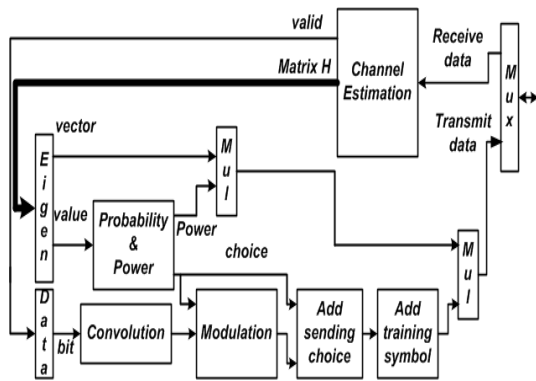
Fig. 3. Transmitter block diagram

The Modulation module shown in Fig.4 uses 4QAM or 16QAM modulation which depends on the input 'choice'. It will be one block 16QAM if the value of 'choice' is zero, and be two blocks 4QAM if the value is one.
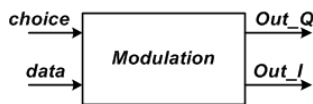

Fig. 4. Modulation module

Each of the signals Out1 and Out2 includes two parts: in-phase (I) and Quadrature (Q) components and is stored in a Look-up table (LUT).

Supposing CSI matrix H is already known, we calculate matrix $H^H H$ and then determine eigenvalues and eigenvectors of the matrix, as shown in Fig. 5. In this module, we use fix-point 10.22 to do all the calculations. Obtained eigenvalues will be converted to single floating-point by module fixed-point to floating-point.
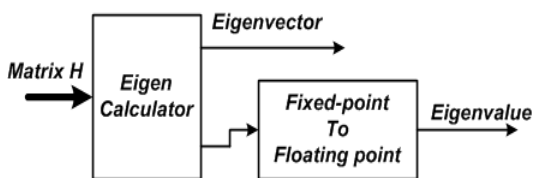

Fig 5. Calculating eigenvalue and eigenvector

In the E-SDM technique, some calculations will give very small values. So, we need to use floating-point to meet the goal of the system. But using floating-point will make the hardware cost be larger than fixed-point. Therefore, we need to use both fixed-point and floating-point in the system.

The most critical part in the system is Calculating power levels and choice values module. In this one, we use floating-point for all calculations because of its wide range. The module has three main parts: calculating power, calculating error-bit probability and deciding to get choice which indicates we need 4QAM or 16QAM modulation. The design is based on results shown in [7]
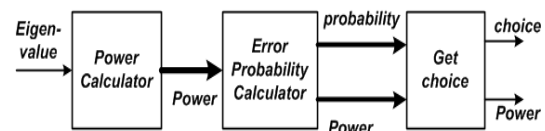

Fig 6. Calculating Power and getting choice

Choice values and training symbols need to be transmitted to RX in order to be able to detect correct transmitted data sub-streams. 'Choice' values is modulated by BPSK and added to the top of the first data stream. The preamble training symbols are added into the original data for channel estimation at the receiver, as shown in Fig.7. Here we use 8 orthogonal Hadamard bits for CSI estimation.
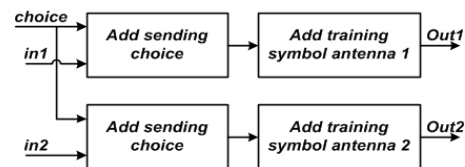

Fig 7. Sending choice and training symbol module
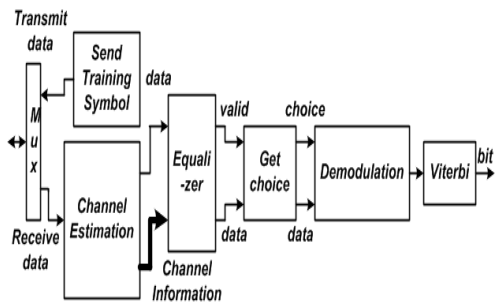
3.2. Receiver side

Fig 8. Receiver Side

The receiver consists of six main parts: add training symbols Rx, channel estimation Rx, decoding, receive choice, choice decision, and demodulation, as shown in Fig. 8.

In next module, we use Zero Forcing to detect receive signals. Here we need two blocks: one when choice is zero, the number of data stream is one 16QAM stream, and two when choice is 1, and the number of data streams is two QPSK streams.
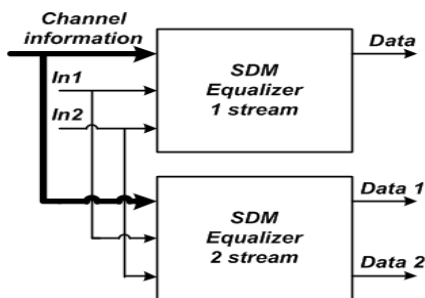

Fig. 9. Equalization module

At Fig.10, we can see the receiving choice module. After decoding, the first data symbol which is modulated with BPSK method contains exactly the choice value we need. So that the receiving choice module will start to demodulate this symbol and get the choice back.
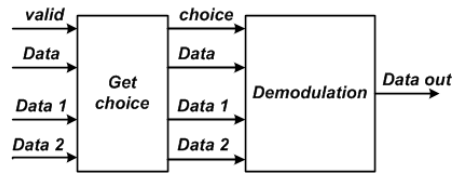

Fig. 10. Getting choice and demodulating module

After getting the choice value, based on it, received signals will be demodulated correctly and get transmitted data.

4. IMPLEMENTED RESULTS AND DISCUSSION

Based on the design and implementation of the MIMO E-SDM systems, in the section, we will evaluate the bit-error rate (BER) of the systems, and compare it with simulation results in Matlab. In the section, we also consider about the hardware consumptions for our system design.

4.1. BER performance of designed systems

The BER performance of 2x2 and 2x3 MIMO E-SDM systems is shown in this section. Here we use zero-forcing weights to detect receive signals. Both channel coding and without channel coding are considered. In the figure, we also want to compare the performance of MIMO E-SDM systems with MIMO SDM systems based on both computer simulation and hardware implementation results. The computer simulation results are obtained by using Matlab software.

Firstly, a comparison of BER performance of MIMO E-SDM systems between computer simulation using Matlab software and implementation results is shown in Fig. 10. Here, we can see that both curves are almost the same. The good match is because we use 32-bit floating point to do all the calculations. This can conclude

that our design and implementation of the systems are correctly.

Secondly, a comparison of BER performance between MIMO E-SDM and MIMO SDM systems is considered in Fig. 11. It can be seen that MIMO E-SDM systems give much better performance than MIMO SDM ones. This is

because of the optimal allocation of transmit data resources and using orthogonal transmit beams in the E-SDM technique. When increasing the number of receive antennas, the BER performance of both MIMO E-SDM and SDM systems is obtained better. This is due to higher diversity gain.
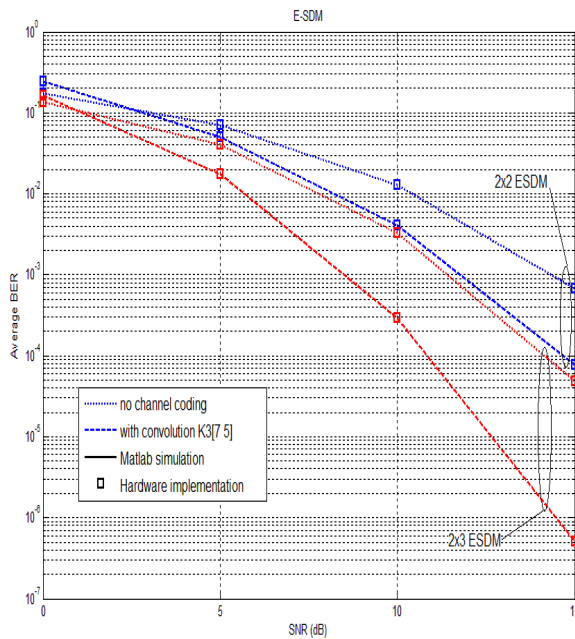

Fig. 10. Comparison between computer simulation and hardware implementation

Fig. 11. Hardware performance of MIMO SDM

4.2. Hardware Cost

In the section, we want to evaluate hardware consumption in our system design and compare it between MIMO E-SDM and MIMO SDM systems.

Table 1 shows the detail hardware consumption of the design of 2x2 MIMO E-SDM system with channel coding. The FPGA device used is Stratix III 3SL150F1152C2. It can be seen from Table 1 that hardware resource can be free approximately

30%. Maximum speed of the system is 145.37 MHz.

The detail hardware consumption of 2x3 MIMO E-SDM system is shown in Table 2. The system occupies about 75% resource and the maximum speed can go upto 142 MHz. It is easy to understand because the 2x3 system needs one more antenna at receiver. That means it needs more hardware to control that antenna and to calculate in the equalizer module. In return, better

BER performance is gotten as seen in Fig 11.

A comparison of the hardware consumption between MIMO E-SDM and MIMO SDM systems is shown in Table 3. As we can see, the hardware cost of E-SDM system is two times larger than SDM. This is because of the much higher calculation in the E-SDM technique. In addition. Table 4 shows all mathematical functions we use in the systems and its number of pipeline stage. It can be seen that the E-SDM technique needs many special kinds of mathematical functions which are very hard to design on Verilog HDL description.

Table1. Hardware Consumptions of 2x2 MIMO E-SDM System

Blocks	Consumption			
	Quantity	Speed (MHz)	ALUTs Max: 113,600	Logic Registers Max: 113,600
Normalize	1	208	588 (<1%)	780 (<1%)
Calculating $H^H H$	1	165	1,285 (1%)	2,071 (2%)
Get eigen-value	1	310	843 (<1%)	2,007 (2%)
Get eigen-vector	1	178	8,451 (7%)	9,636 (8%)
Get choice	1	418	95 (<1%)	127 (<1%)
Calculating Power	1	217	8,988 (8%)	11,468 (10%)
Calculating Probability	1	203	4182 (4%)	6557 (6%)
Channel Estimation	2	147	3,530 (3%)	7,505 (7%)
Sending choice	1	401	4 (<1%)	129 (<1%)
Add training symbol	4	243	15 (<1%)	74 (<1%)
Choice decide	1	420	128 (<1%)	194 (<1%)
SDM decoder 2 stream	1	162	22,519 (20%)	19,596 (17%)
SDM decoder 1 stream	1	169	9,232 (8%)	7,392 (7%)
Receiving choice	1	382	21 (<1%)	10 (<1%)
Total evaluation		145	<55%	<69%

Table2. Hardware Consumptions of 2x3 MIMO E-SDM System

Blocks	Consumption			
	Quantity	Speed (MHz)	ALUTs Max: 113,600	Logic Registers Max: 113,600
Modulation	1	420	27 (<1%)	10 (<1%)
Normalize	1	208	588 (<1%)	780 (<1%)
Transmit	1	167	1,297 (1%)	1,824 (2%)
Calculating $H^H H$	1	162	2,259 (2%)	4,279 4%)
Get eigen-value	1	310	843 (<1%)	2,007 (2%)

Get eigen-vector	1	178	8,451 (7%)	9,636 (8%)
Get choice	1	418	95 (<1%)	127 (<1%)
Calculating Power	1	217.53	8,988 (8%)	11,468 (10%)
Calculating Probability	1	203	4182 (4%)	6557 (6%)
Channel Estimation	2	147	4,181 (4%)	9,520 (8%)
Add training symbol Tx	5	243	15 (<1%)	74 (<1%)
Choice decide	1	420	128 (<1%)	194 (<1%)
Demodulation	1	420	64 (<1%)	10 (<1%)
SDM decoder 2 stream	1	160	35,462 (31%)	24,212(21%)
SDM decoder 1 stream	1	165	10,526 (9%)	8,109 (7%)
Receiving choice	1	382	21 (<1%)	10 (<1%)
Total evaluation		142	<70%	<75%

Table3. Comparing Hardware Consumptions between MIMO Systems

MIMO	Consumption		
	Max Speed (MHz)	ALUTs Max: 113,600	Logic Registers Max: 113,600
SDM 2x2	147	30%	31%
E-SDM 2x2	145	55%	69%
SDM 2x3	147	43%	36%
E-SDM 2x3	142	70%	75%

Table 4. Mathematical Functions for Real Numbers

Mathematical Function	The number of Pipeline Stages
Addition, Subtraction	8
Multiplication	4
Division	43
Square root	24
Logarithmic function	18
Exponential function	29

5. CONCLUSION

MIMO systems applying the E-SDM technique have been considered as a potential technology for future broadband wireless communications because of having maximum channel capacity. In the paper, we have shown our own design and implementation of two MIMO E-SDM systems on hardware of FPGA-based DSP

Development Kit. Results of BER performance of the systems have shown that our design is good and reliability. We also compare the performance of MIMO E-SDM systems with MIMO SDM systems. It has shown an outperformance of MIMO E-SDM systems. In the paper, we also calculate the consumption of FPGA elements in our design. For 2x2 MIMO system, the hardware resource can be free approximately 30%.

When compared with MIMO-OFDM E-SDM system in [15], the hardware resource of Indoor MIMO E-SDM systems is much more smaller. 5% free cost of 2x2 OFDM system is consequence of this complexity in this system. In this case, we need to calculate TX weight matrix and estimate RX weight matrix in each carrier. Therefore, it is very hard to control data flow. In addition, we need FFT and IFFT module in the MIMO-OFDM E-SDM to prevent multi-paths. However, to estimate Channel and RX weight matrix, the system need both FFT and IFFT modules in each side, transmitter and receiver. In [15], we design a module which can transform between FFT and IFFT to decrease hardware resource.

Thực thi hệ thống MIMO E-SDM cho mạng không dây tương lai trên FPGA

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TÓM TẮT:

Các hệ thống Multiple-input multiple-output (MIMO) áp dụng kỹ thuật Eigenbeam-Space Division Multiplexing (E-SDM) có thể được xem như các hệ thống MIMO tối ưu vì có thể mang lại dung lượng kênh cao nhất và độ tin cậy cao. Trong các hệ thống này, các luồng dữ liệu trực giao được truyền đi giữa hai bên phát và thu, và các dữ liệu truyền đầu vào sẽ được phân bổ hợp lý. Bên cạnh đó, tại phía thu, một bộ tách tín hiệu đơn giản sẽ được dùng để loại bỏ nhiễu giữa các luồng. Chính vì thế, các hệ thống MIMO E-SDM được xem là công nghệ tiềm tàng cho các kết nối mạng tốc độ cao trong tương lai. Mặc dù có rất nhiều tài liệu kĩ thuật đã ước lượng các hệ thống này trên phép phân tích học thuyết hay mô phỏng, nhưng hầu như rất ít bài báo mô tả việc thiết kế hệ thống MIMO E-SDM trên phần

cứng. Mục đích chính của bài báo này là mô tả thiết kế và thực thi các hệ thống MIMO E-SDM 2x2 và 2x3 trên kit phát triển của Altera bằng cách dùng ngôn ngữ thiết kế phần cứng Verilog HDL. Lỗi bit của hệ thống và độ tiêu tốn tài nguyên của hệ thống cũng được đưa ra để cho thấy tính tin cậy của các thiết kế này.

Từ khóa: MIMO, E-SDM, ZF, FPGA, hardware design.

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