

New space vector PWM method based on virtual flux vector for T-NPC Inverter

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ABSTRACT

This paper proposes a new SVPWM algorithm for operating the three-level TNPC topology. The idea of this algorithm is approximating as close as possible the locus of actual virtual flux vector and ideal one and minimizing the numbers of switching in one switching interval to improve the efficiency of the whole system. The virtual flux vector is

monitored to determine the sector and the proper non-zero voltage vectors. The performance of the converter and the comparison of different modulation methods are analyzed. Simulation and experimental results show that the proposed method provides high efficiency.

Keywords: *Multilevel, NPC, T-NPC, SVPWM, switching losses, Virtual Flux Vector.*

1. INTRODUCTION

In recent years, the multilevel converters topologies were introduced, especially the three-level neutral-point-clamped (NPC) topology because it has many significant advantages [1]-[4]. Some studies are implemented to compare between three-level inverters and two-level inverters for low voltage and low power applications and the three-level inverters have more attraction [3]. They have some advantages such as: the reduction of voltage blocked by each semiconductor, high efficiency of the power converter and low total harmonic distortion of output voltage.

The three – level NPC can be classified into three types: the conventional NPC [2], the active NPC (A-NPC) [5] and the T-type NPC (T-NPC) [6].

- The conventional NPC topology has 12 IGBTs and 6 anti-parallel free-wheeling diodes in three legs. The DC-link is split in two symmetric halves connected in series. In NPC topology every conduction path consists of two semiconductors in series and it can either handle higher DC-link voltages or the blocking voltage of the switches can be reduced in comparison to a two-level converter topology [1], [2].

- The active NPC topology is a derivative of the conventional NPC, 6 anti-parallel free-wheeling diodes are replaced by 6 IGBTs [5]. Compared with a typical three-level neutral-point-clamped converter, the recent studies proposed that three-level active neutral-point-clamped (A-NPC) converter can overcome the unequal loss distribution among semiconductor devices. However, this converter has some drawbacks such as: the increased number of power semiconductor devices and low efficiency.

- The T-NPC topology is showed in Fig. 1. This is a new topology which can overcome the disadvantages of conventional NPC and A-NPC. Each leg of the T-NPC consists of four power devices: the S1 and S4 is connected series with DC power supply and one bidirectional switch (S2 and S3) which connect the middle point of three legs to the middle point of DC-link. This topology is simpler than the conventional NPC and A-NPC because it has less semiconductor devices. The T-NPC provides some advantages that are not available in conventional NPC such as: low conduction losses, fewer numbers of power switches, small size and simple operation. Therefore, in the low voltage range, from 500V to 1000V with the requirement of high efficiency and high power, instead using the two-level

inverter and the conventional three-level NPC, the T-NPC is the applicable solution. Especially, in the solar energy conversion systems, the efficiency is the important factor.

The PWM algorithms for T-NPC are also investigated in recent technical publications.

The carrier based pulse width modulation (PWM) with third harmonics injection and can be applied for the T-NPC inverter [7]. This modulation method is simple because it is based on the intersection between the modulation signals and high frequency carrier signal to generate the gating pulses for power switches. However, the high switching losses and THD are the disadvantages of this method. The space vector PWM (SVPWM) technique with their inherent advantage as it gives a higher output voltage for the same DC bus voltage, reduced loss and better harmonic performance for three-phase VSI. The SVPWM was introduced in order to obtain the optimal number of switching [8]. However, the selection of proper active and zero vectors to synthesis the reference output voltage vectors is very complex. The SVPWM 3L-2L method is based on the SVPWM of conventional two-level inverter, it is more simple than the traditional SVPWM [9].

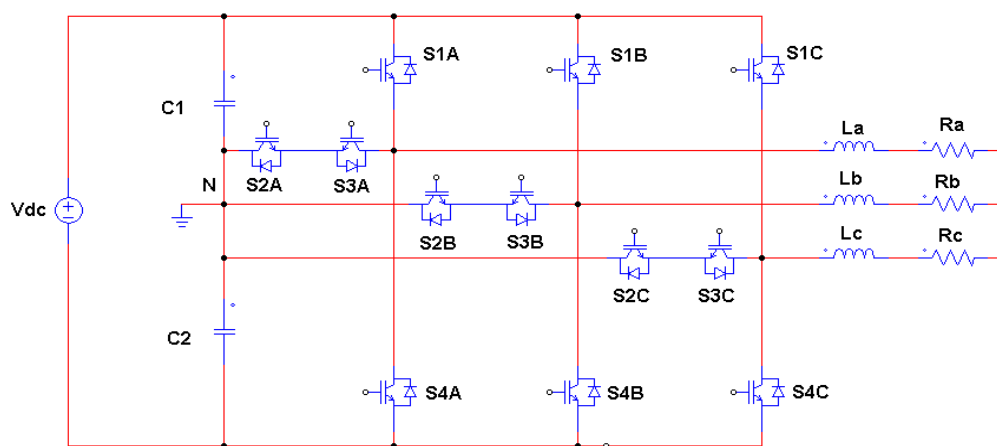


Fig.1. The configuration of the three-level T-NPC

This paper proposed a new SVPWM algorithm which is based on locus analysis of the virtual flux vector. The proposed SVPWM has some advantages such as: simple computation, minimization of switching losses and high performance output voltage. Therefore, the T-NPC with the proposed method is suitable such as in photovoltaic applications for low-voltage range.

The structure of T-NPC and the proposed SVPWM algorithm are expressed clearly in this paper. The simulation and experimental results are also expressed to demonstrate the feasibility of this algorithm.

2. THE PRINCIPLE OPERATION OF T-NPC AND THE SPACE VECTOR ANALYSIS

The three-phase three-level T-NPC topology is illustrated in Fig. 2. Beside the conventional two-

level voltage source inverter topology, an active bidirectional switch is added to each phase leg, connecting to the DC-link voltage midpoint. The bidirectional switches are used to isolate the inverter part from the grid while the zero state is applied. Unlike the switches S1 and S4, the bidirectional switch (S2 and S3) has to block only half of the dc-link voltage. For low voltage application, switches S1 and S4 will be implemented with 1200V IGBT/diodes while S2 and S3 need only a 600V switch.

The switching state of the power switches and the output voltage of the T-NPC are shown in Table I. There are 3 levels of phase to common point voltage that can be generated on each phase leg: +E , 0, -E, where E is the voltage of each capacitor.

For state +E and -E, the current direction go through the system as shown in Fig. 2a.

Table 1. Switching state and output voltage of each phase

Switching State	Switching Status				Output Voltage V_{AN}
	S1	S4	S2	S3	
+1	ON	OFF	ON	OFF	E
0	OFF	OFF	ON	ON	0
-1	OFF	ON	OFF	ON	-E

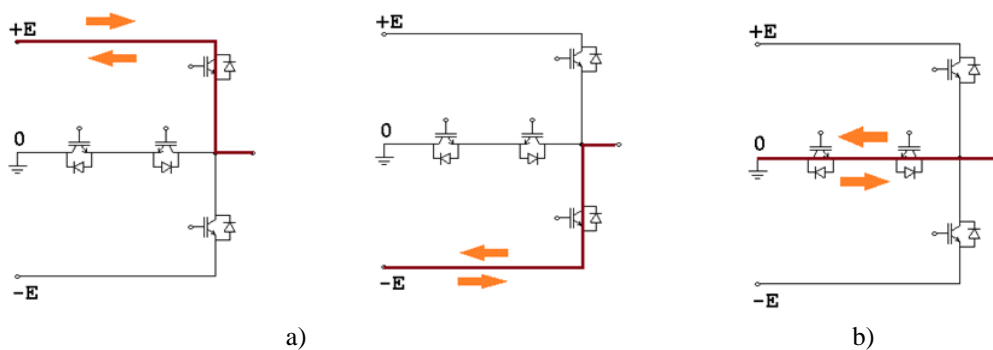


Fig.2. (a) Current direction during state + E and -E
(b) Current direction during zero state

For zero state, the current will not pass through the inverter but the bidirectional switches to return to the load as shown in Fig.2b.

The SVM is a pulse width modulation strategy that uses the concept of space vectors to compute the duty cycles of the switches. To implement this modulation strategy to the T-NPC, the output phase voltages generated by the switching states of the T-NPC have to be converted into space vectors using the following transformation:

$$\vec{V} = V_a(t) + V_b(t)e^{j\frac{2\pi}{3}} + V_c(t)e^{j\frac{4\pi}{3}} \quad (1)$$

Where $V_a(t)$, $V_b(t)$, $V_c(t)$: instantaneous phase voltages ; j : complex number

Fig.3 shows the space vector diagram of the NPC in the $\alpha\beta$ coordinate system that is formed by the voltage space vectors which includes four

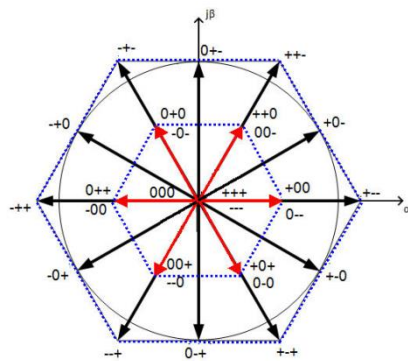


Fig. 3. Space vectors of a T-NPC in $\alpha\beta$ coordinate system

3. THE PROPOSED SVPWM METHOD BASED ON THE VIRTUAL FLUX VECTOR

The proposed algorithm aims to minimize the number of switching of the switches, which conclude in power loss reduction and to approximate as close as possible the locus of actual virtual flux vector and ideal one. Its idea is based on analyzing the flux linkage vector of the

groups accordingly with 27 switching states: zero voltage vectors, small voltage vectors, medium voltage vectors, large voltage vectors.

SVPWM is a technique that creates IGBT signal pulses from generating the appropriate reference space vector which corresponds to a combination of switching states of three phase legs. The intervals of each state in a switching cycle are calculated depending on the sector where locates the desired space vector.

$$T_s \cdot \vec{V} = T_x \vec{V}_x + T_y \vec{V}_y + T_z \vec{V}_z \quad (2)$$

$$T_s = T_x + T_y + T_z$$

where T_x , T_y and T_z are intervals of two active output vectors V_x , V_y and zero vector V_z , respectively.

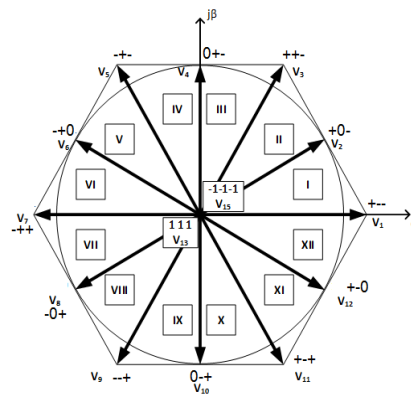


Fig. 4. The sector division of the proposed method

3 phase asynchronous motor. However, for other loads, the virtual vector concept can be used regarding the analogy between them and the three-phase AC machine. The virtual flux vector is defined as follows:

$$\Psi^*(t) = \int_0^t V(t) = -\frac{3}{2} \frac{U_m}{\omega} e^{j\omega t} + \Psi_0^* \quad (3)$$

U_m – amplitude of output phase voltage; ω - angular velocity of phase voltage vector, Ψ_0^* - initial value of virtual flux vector.

In ideal conditions, the flux vector describes a circle whose radius equals to $\frac{3U_m}{2\omega}$ and moves under the similar angular velocity of the voltage vector. The voltage vector is tangent to this circle. By applying necessary non-zero voltage vectors, a quasi circle will be created.

The locus of the flux linkage vector is as first divided in small arcs dx , each corresponds to the angle $\omega \cdot \Delta T$ that scans the flux vector during a switching time. The reference virtual flux vectors and voltage vectors will be controlled by 2 non-zero vectors and 1 zero vector.

The $\alpha\beta$ plan is now divided to 12 zones with 12 non-zero large and medium vectors and 2 zero vectors (Fig.4).

According to the phase angle of the reference vector, two appropriate non-zero base voltage vectors (V_n, V_{n+1}) will be chosen. Their order of formation is calculated in such way so that for each change of switching states, only one switch changes its status, which ensures the safety and minimization of switching losses. In addition, the symmetrical arrangement of base space vectors aims to decrease the discrepancy between the formed quasi-circular locus and the desired circular one. This approach ensures the best approximation of actual flux vector to ideal one in order to achieve the best quality, i.e. the lowest of total harmonic distortion of output voltage vector.

Besides that, in the PV system, due to high modulation index, the use of small vector in SVPWM does not necessarily. So, the rule of applying switching states is then presented as follows: *Zero Vector – Large Vector – Medium Vector – Large Vector – Zero Vector*.

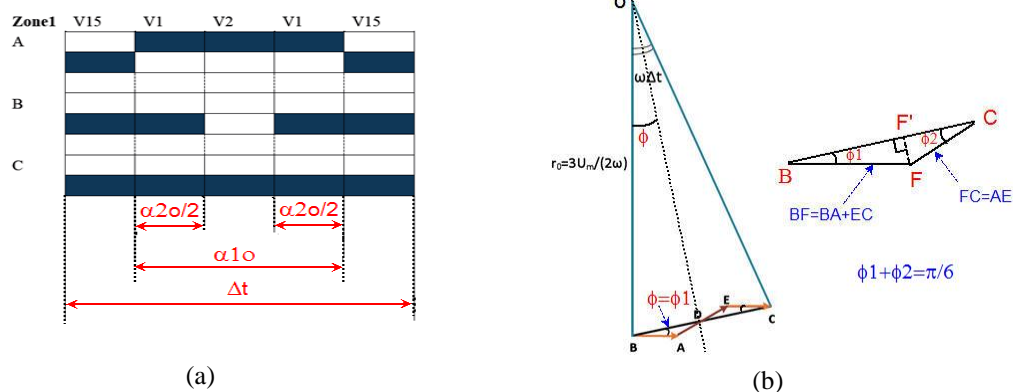


Fig. 5.(a) Pulse pattern and definition of $\alpha_{1_odd}, \alpha_{2_odd}$ in sector I
(b) Computing geometrically the reference output voltage vector in sector I

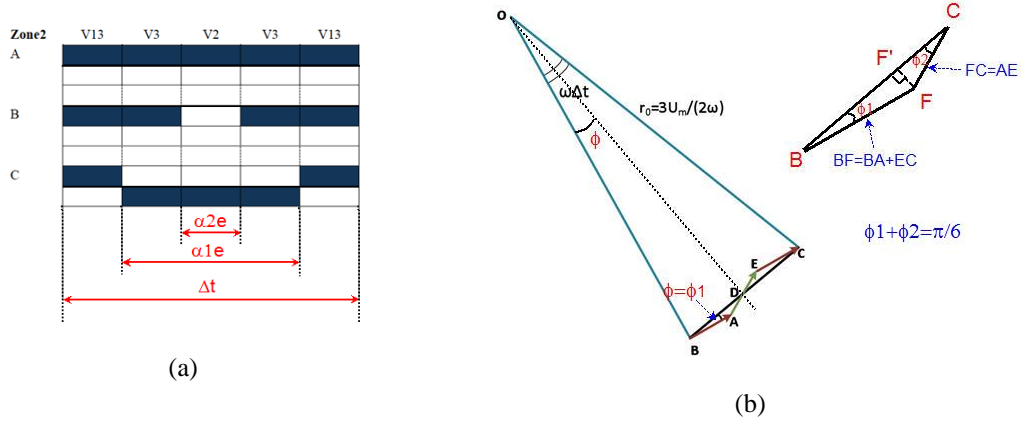


Fig.6. (a) Pulse pattern and definition of α_{1_even} , α_{2_even} in sector II

(b) Computing geometrically the reference output voltage vector in sector II

In order to reduce the switching loss, the pulse pattern is combined so that the one leg maintains the state +E or -E over the whole switching period ΔT (for example phase C in Fig.5a and phase A in fig.6a).

For duration calculation, after determining the sector that contains the reference voltage, it is necessary to decide the suitable formula whether the sector indication is even or odd. For odd sectors, e.g. sector I, the virtual flux vector is controlled by 2 vectors \vec{V}_1 and \vec{V}_2 . The desired pulse pattern is presented in the Fig. 5a.

By computing the two values α_{1o} , α_{2o} , the duration corresponding to each vector could be found. Assuming the angle is small enough due to high switching frequency of switches, the arc (BC) is considered as the segment BC.

Considering the triangle OBC in Fig. 5b, the side BC can easily be calculated:

$$BC = 2 \times \frac{3U_m}{2\omega} \times \sin\left(\frac{\omega \cdot \Delta T}{2}\right) \approx \frac{3U_m}{\omega} \times \frac{\omega \Delta T}{2} = \frac{3}{2} U_m \Delta T \quad (4)$$

$$U_m = M \times \frac{\sqrt{3}}{2} U_d \times \frac{2}{3} = \frac{U_d}{\sqrt{3}} \quad (5)$$

$$BC = \frac{\sqrt{3}}{2} M U_d \Delta T \quad (6)$$

where M - the modulation index, $U_d = 2E$ - the DC link voltage.

In the triangle ABD and BFC as Fig. 5b, because of the symmetrical distribution of the pulse pattern, we can find that:

$$BD = \frac{1}{2} BC; BC = BF' + F'C \quad (7)$$

$$BA = EC = \frac{BF}{2}; AD = DE = \frac{FC}{2}$$

and two sides BF, FC are successively:

$$BF = \alpha_{1o} \cdot |\vec{V}_1| = \alpha_{1o} \cdot U_d$$

$$FC = (\alpha_{1o} - \alpha_{2o}) \cdot |\vec{V}_2| = (\alpha_{1o} - \alpha_{2o}) \cdot \frac{\sqrt{3}}{2} \cdot |\vec{V}_1| = (\alpha_{1o} - \alpha_{2o}) \cdot \frac{\sqrt{3}}{2} \cdot U_d \quad (8)$$

The simultaneous equations are then established for one switching period by using (6)-(8):

$$BF \cdot \cos \phi_1 + FC \cdot \cos \phi_2 = BC$$

$$\Leftrightarrow \alpha_{2o} U_d \cos \phi + (\alpha_{1o} - \alpha_{2o}) \frac{\sqrt{3}}{2} U_d \cos\left(\frac{\pi}{6} - \phi\right) = \frac{\sqrt{3}}{2} M \cdot U_d \cdot \Delta T \quad (9)$$

$$BF \cdot \sin \varphi_1 = FC \cdot \sin \varphi_2 = FF' \quad (10)$$

$$\Leftrightarrow \alpha_{2o} U_d \sin \varphi = (\alpha_{1o} - \alpha_{2o}) \frac{\sqrt{3}}{2} U_d \sin \left(\frac{\pi}{6} - \varphi \right)$$

Resolving the simultaneous equations (9)-(10), we get the calculation formula of intervals α_{1o} and α_{2o} in each switching period ΔT :

$$\alpha_{1o} = M \cdot \Delta T \cdot \cos \left(\varphi - \frac{\pi}{6} \right) \quad (11)$$

$$\alpha_{2o} = \sqrt{3} \cdot M \cdot \Delta T \cdot \cos \left(\varphi + \frac{\pi}{3} \right)$$

Similarly, in even sectors, e.g. sector II, the intervals α_{1e} and α_{2e} , as described in Fig.6a, are defined as follows, according to the geometrical analyze in Fig.6b:

$$\alpha_{2e} \frac{\sqrt{3}}{2} U_d \cos \varphi + (\alpha_{1e} - \alpha_{2e}) U_d \cos \left(\frac{\pi}{6} - \varphi \right) = \frac{\sqrt{3}}{2} M \cdot U_d \cdot \Delta T$$

$$\alpha_{2e} \frac{\sqrt{3}}{2} U_d \sin \varphi = (\alpha_{1e} - \alpha_{2e}) U_d \sin \left(\frac{\pi}{6} - \varphi \right) \quad (12)$$

Resolving the simultaneous equations, we get the calculation formula of intervals α_{1e} and α_{2e} in each switching period ΔT :

$$\alpha_{1e} = M \cdot \Delta T \cdot \cos \varphi \quad (13)$$

$$\alpha_{2e} = 2 \cdot M \cdot \Delta T \cdot \cos \left(\varphi + \frac{\pi}{3} \right)$$

The pulse patterns for proposed SVPWM for remaining sectors are shown in Fig. 7.

Semiconductor losses in voltage source IGBT converters can be calculated using method in [10]. The efficiency of the T-NPC is calculated by the formula:

$$\eta = \frac{P_{out}}{P_{in}} \quad (14)$$

where P_{in} is the input DC power, P_{out} is the output AC power according to 1st voltage harmonic:

$$P_{in} = V_{dc} I_d \quad (15)$$

$$P_{out} = P_{in} - P_{losses} \quad (16)$$

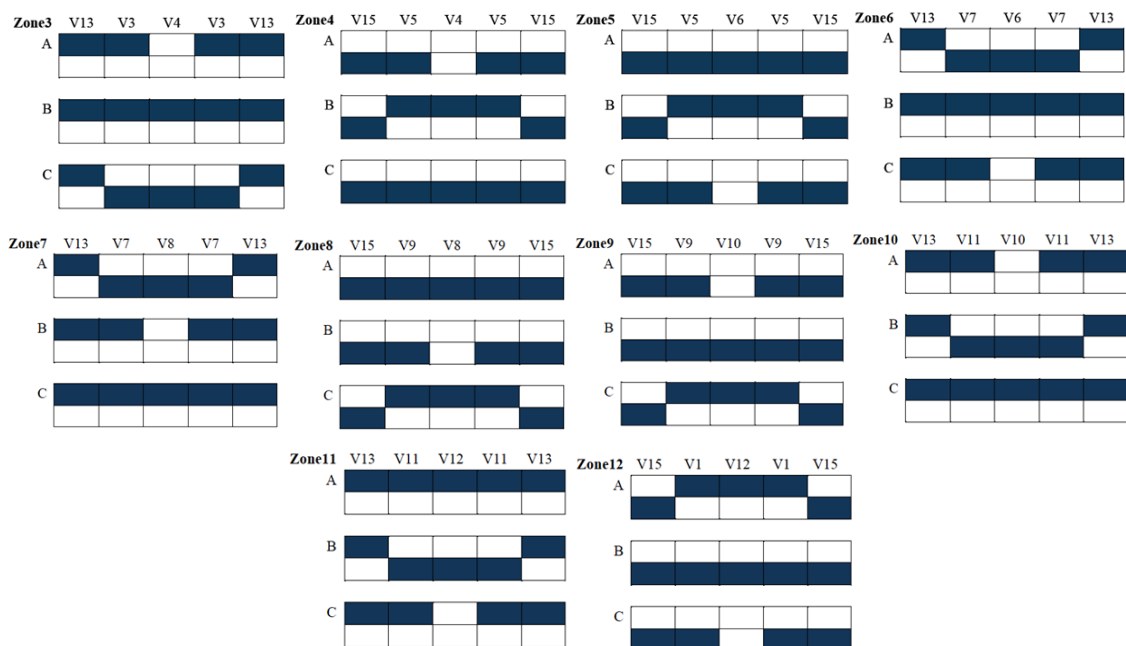


Fig. 7. The switching pattern for sector (zone) from 3 to 12

4. SIMULATION RESULTS

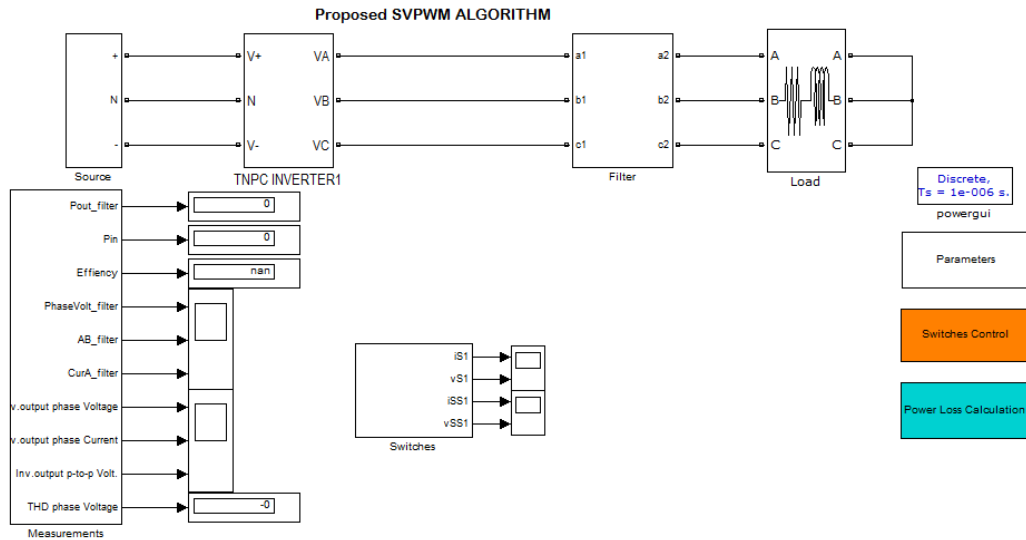
Simulation model is carried out by Matlab/Simulink software to verify the proposed SVPWM method (Fig.8). The system model is simulated with the parameters as follows:

- The dc-link voltage is 800 V (E=400V)

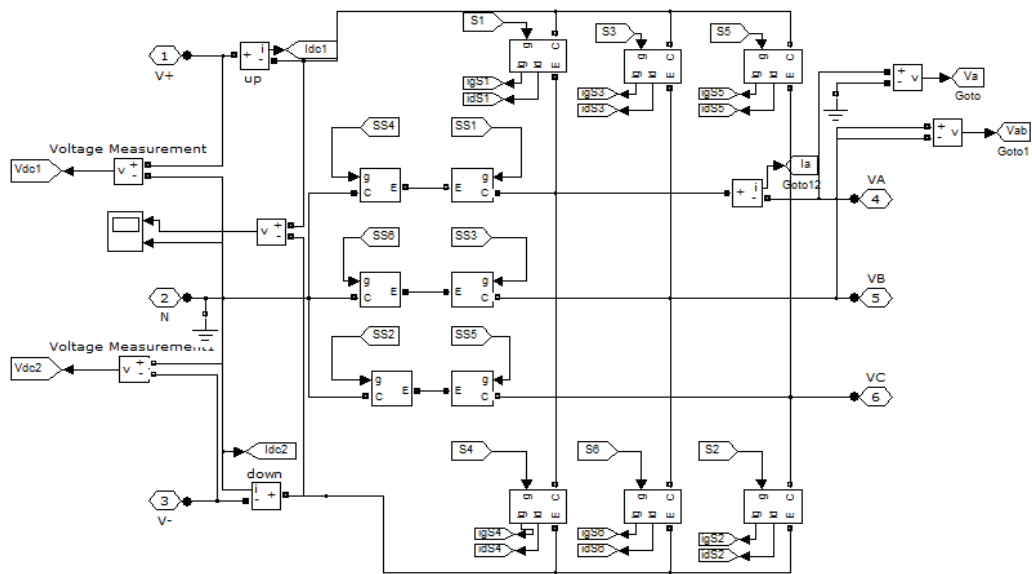
- The three-phase RL load $R= 20 \Omega$ $L = 5$ mH.

- The L Filter : $L = 0.2$ mH, $R = 0.01 \Omega$

- Switch parameters: IGBT resistor on = 0.016Ω , IGBT forward voltage = 2.25V, Diode resistor on = 0.016Ω , Diode forward voltage = 0.9V



a) System simulation model



b) T-NPC inverter model

Fig.8. Simulation model of T-NPC inverter with the proposed SVPWM method

Fig. 9 shows the simulation PWM signals for four power switches of leg A. We can see that in each sector, there is at least one switch which does not change the state. Therefore, the number of switching is reduced.

The phase and line-to-line output voltage are shown in Fig. 10 and 11, respectively. With the switching frequency is 4.8 kHz and the

modulation index is 0.8, the number of switching is 96. It can be seen that the line-to-line output voltage has five values: -800V, -400V, 0V, 400V, 800V.

The filtered phase, line-to-line output voltage and output current are shown in Fig. 12 and 13, respectively. The pure sinusoidal output current is obtained with the proposed method.

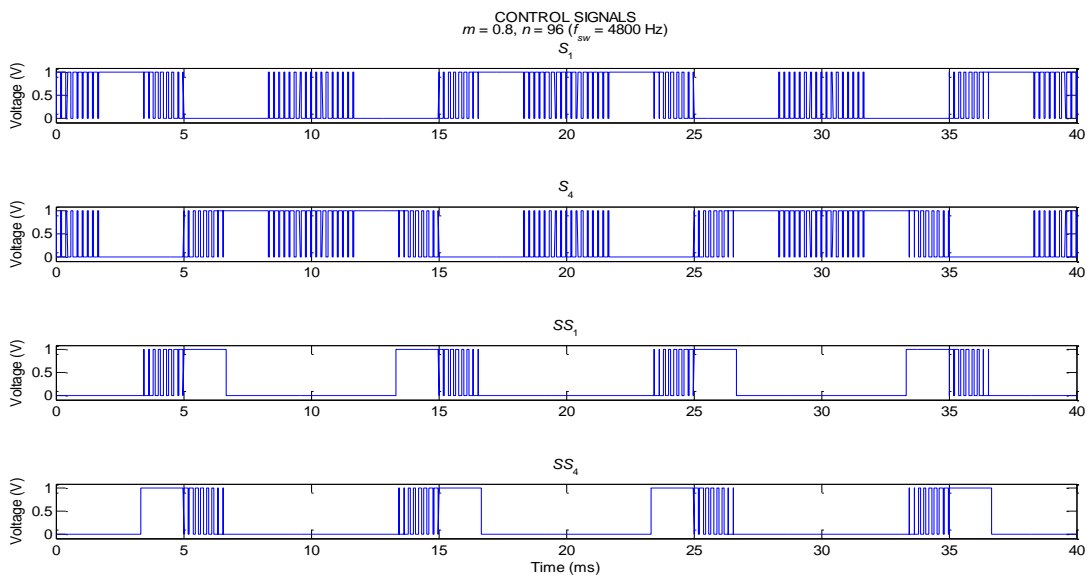


Fig.9. Switching signals for four power switches of leg A

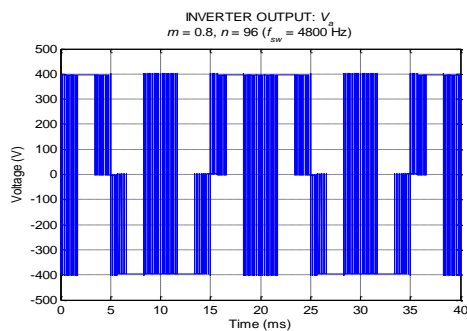


Fig.10. The phase output voltage waveform

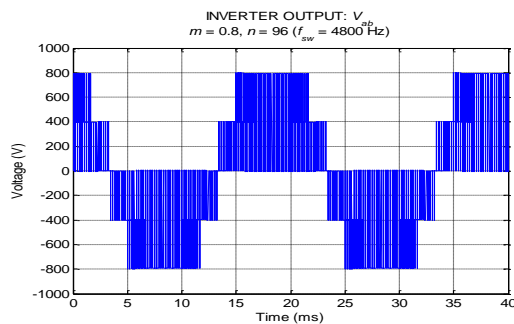


Fig.11. The line-to-line output voltage waveform

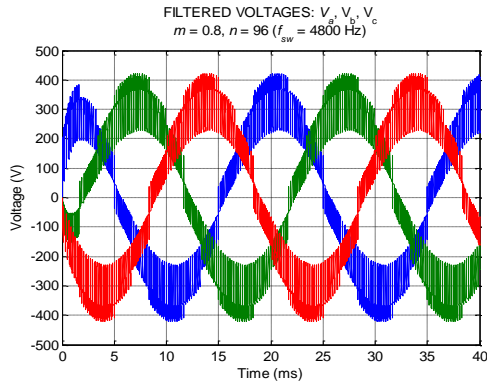


Fig.12. The filtered phase voltage waveforms

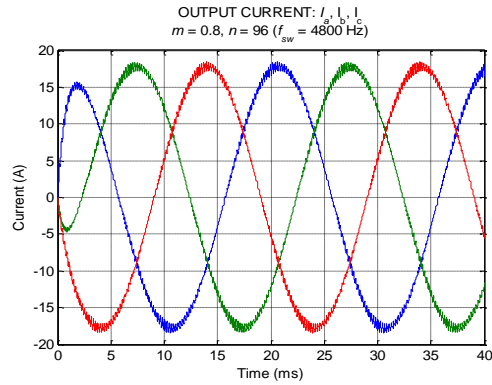


Fig. 13. The phase output current waveforms

Table 2. The data comparison result between the proposed SVPWM method, spwm (SFO- SINPWM with triple harmonics) & conventional SVPWM methods

P _{load} (W)	1290-1300		
	SPWM (SFO)	SVPWM [9]	Proposed SVPWM
V _{A1} (phase), [V]	140.6	141.6	141.4
V _{A1} (filtered), [V]	131.2	131.7	131.6
I _{A1} (filtered), [A]	6.539	6.564	6.561
P _{in} , [W]	1326	1338	1334
P _{loss} , [W]	31.88	32.14	25.59
P _{out} , [W]	1294.12	1305.86	1308.41
Efficiency, [%]	97.6	97.6	98.08

Table 3. The efficiency comparison result between the proposed SVPWM method, SPWM (SFO) & SVPWM methods [9]

P _{load} (W)	700	900	1300
Method	Efficiency (P _{out} /P _{in}), [%]		
SPWM (SFO)	97.29	97.46	97.6
SVPWM [9]	97.3	97.47	97.6
Proposed SVPWM	97.89	97.99	98.08

In order to show the effectiveness of the proposed SVPWM method, the efficiency of the T-NPC is the main factor to compare different modulation methods.

Table 2 shows the electrical data of the T-NPC with SPWM, conventional SVPWM and proposed SVPWM methods (V_d=320VDC,

f_{sw}=10kHz, f₁=50Hz, Filter R_f=0.01Ω, L_f=20mH, Load R_L=20Ω, L_L=5mH, P_{load} = 1290-1300W).

Table 3 shows the efficiency for different values of power load for the T-NPC with SPWM, typical SVPWM and proposed SVPWM methods (V_d=320VDC, f_{sw}=10kHz, f₁=50Hz, Filter R_f=0.01Ω, L_f=20mH, Load R_L=20Ω, L_L=5mH).

It can be seen that the proposed SVPWM method provides higher efficiency as compared to SPWM and conventional SVPWM methods.

5. EXPERIMENTAL RESULTS

To validate the proposed SVPWM method and simulated results, an experimental platform is setup in the laboratory. The experimental prototype is shown in Fig.14. The half-bridge IGBT Modules SEMiX202GB128Ds (1200V) were selected for switch pairs: (S1A,S4A), (S1B,S4B) and (S1C,S4C) while the bi-direction IGBT modules SK60GM123 (1200V) were chosen for the switch pairs (S5A,S6A), (S5B,S6B) and (S5C,S6C). These IGBT modules is the new generation IGBT from Semikron and exhibit good characteristics for minimizing both switching and conduction losses. They are a good option for making the prototype operate with high voltage input and high power (800V DC, 10kW). By using pulse transformers, gate driver for these IGBT modules are isolated from the secondary side, which operates under high voltage. Furthermore, the gate drivers can protect the inverter from short circuit condition, thus the inverter can operate safety while testing algorithms under high voltage. The prototype is controlled by a high performance, floating point digital signal processor (DSP) 90MHz TMS320F28069 from Texas Instruments. An isolated 5V source is designed for supplying power for the DSP.

The experimental parameters are as follows:

- DC link voltage: 320V
- Switching frequency: 10 kHz
- Three—phase RL load: $R = 10 \Omega$, $L = 5$ mH

Table 2 shows the efficiency of T-NPC inverter with the proposed method and conventional SVPWM method according to the output power. It can be seen that with the proposed method, the higher efficiency is obtained.

Fig. 15 a, b, c and d show the output current, output voltage and gating pulse for switch S1 and S4. The output currents of the T-NPC with proposed methods are sinusoidal waveform and balance.

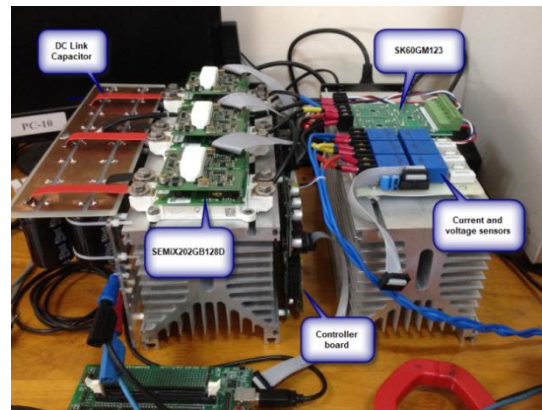


Fig.14. Experimental model

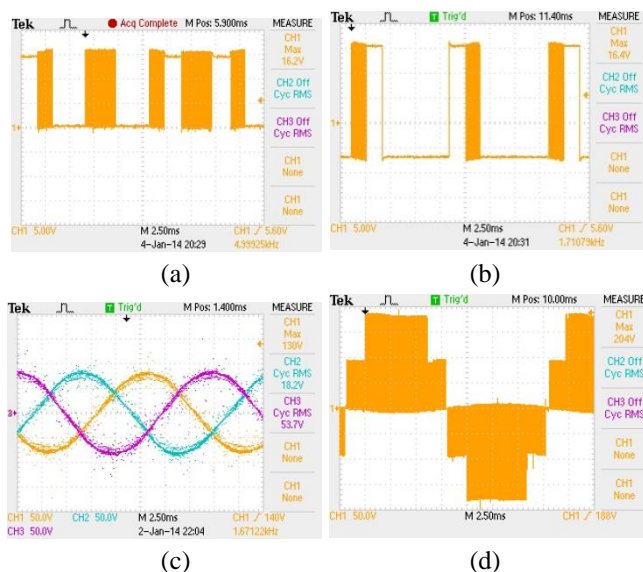


Fig. 15 (a) The three-phase output currents (b) The phase output voltage
 (c) The gate signal for switch S1 (d) The gate signal for switch S4

Table 2. The efficiency comparison between proposed method and conventional method

Output Power	Efficiency		
	Proposed SVPWM	SINPWM (SFO)	Conventional SVPWM [9]
500	94.2	94	93
700	95.5	94.9	94.4
1000	96.4	95.7	95.5
1200	96.8	95.9	95.9
1500	97.2	96.2	96.2
1800	97.3	96.4	96.4

6. CONCLUSION

The T-NPC is an alternative to the two-level VSC for medium switching frequency applications and is very efficient in the range of 4–30 kHz. In this paper, the new SVPWM method is proposed for T-NPC to obtain high efficiency with low-voltage application.

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TÓM TẮT

Bài báo này đề xuất một thuật toán mới cho điều chế vector không gian của cấu hình 3 bậc dạng TNPC. Ý tưởng của thuật toán này là cách tiệm cận quỹ tích véc tơ từ thông ảo thực tế với lý tưởng nhằm đạt chất lượng cao điện áp tổng hợp và tối thiểu hoá số lần đóng cắt trong một chu kỳ đóng cắt để tăng

hiệu suất toàn hệ thống. Vector từ thông ảo được quan sát để xác định sector và các vector điện áp thích hợp. Sự vận hành của bộ biến đổi và kết quả so sánh với các giải thuật điều chế cũng được phân tích. Các kết quả mô phỏng và thực nghiệm chỉ ra rằng giải thuật đề xuất có hiệu suất cao.

Từ khoá: Đa bậc, NPC, T-NPC, SVPWM, tổn hao đóng cắt, từ thông ảo

REFERENCE

- [1]. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no.5, pp. 518–523, Sep. 1981.
- [2]. R. H. Baker, "Bridge converter circuit," U.S. Patent 4 270 163, May 26, 1981.
- [3]. Teichmann, R.; Bernet, S., "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," Industry Applications, IEEE Transactions on , vol.41, no.3, pp.855,865, May-June 2005.
- [4]. Rodriguez, J.; Bernet, S.; Steimer, P.K.; Lizama, I.E., "A Survey on Neutral-Point-Clamped Inverters," Industrial Electronics, IEEE Transactions on , vol.57, no.7, pp.2219,2230, July 2010
- [5]. T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," IEEE Trans. Ind. Electron., vol. 52, no. 3, pp. 855–868, Jun. 2005.
- [6]. Schweizer, M.; Kolar, J.W., "Design and Implementation of a Highly Efficient Three-

- Level T-Type Converter for Low-Voltage Applications," *Power Electronics, IEEE Transactions on* , vol.28, no.2, pp.899,907, Feb. 2013
- [7]. Houldsworth, John A.; Grant, Duncan A., "The Use of Harmonic Distortion to Increase the Output Voltage of a Three-Phase PWM Inverter," *Industry Applications, IEEE Transactions on* , vol.IA-20, no.5, pp.1224,1228, Sept. 1984
- [8]. Kaku, I. Miyashita, and S. Sone, "Switching loss minimised space vector PWM method for IGBT three-level inverter," *IEE Proc. Electr. Power Appl.*, vol. 144, no. 3, pp. 182–190, May 1997.
- [9]. Jae-Hyeong Suh; Chang-Ho Choi; Dong-Seok Hyun, "A new simplified space-vector PWM method for three-level inverters," *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual* , vol.1, no., pp.515,520 vol.1, 14-18 Mar 1999
- [10]. Bierhoff, M.H.; Fuchs, F.W., "Semiconductor losses in voltage source and current source IGBT converters based on analytical derivation," *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual* , vol.4, no., pp.2836-2842 Vol.4, 2004