IMPROVEMENT OF SHORT CIRCUIT CURRENT OF MONO CRYSTALLINE SILICON SOLAR CELLS

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ABSTRACT: *In this report we present series of experiments during which the short circuit current of mono crystalline silicon solar cell was improved step by step so as a consequence the efficiency was increased. At first, the front contact of solar cell was optimized to reduce the shadow loss and the series resistance. Then surface treatments were prepared by TMAH solution to reduce the total light reflectance and to improve the light trapping effect. Finally, antireflection coatings were deposited to passivate the front surface either by silicon nitride thin layer or to increase the collection probability by indium tin oxide layer, and to reduce the reflectance of light. As a result, solar cells of about 13% have been obtained, with the average open circuit voltage V_{oc} about 527mV, with the fill factor about 68% and the short circuit current about 7.92 mA/cm^2 under the irradiation density of 21 mW/cm^2.*

Keywords: *monocrystalline silicon solar cell, front contact, anti-reflection coating.*

1. INTRODUCTION

Since the first modern photovoltaic cell was developed in 1954 at Bell Laboratories with 6% of efficiency, many research in crystalline silicon technologies have been carried out giving great developments of monocrystalline solar cell efficiency. However, in Vietnam there were few research and applications in solar cell technologies, which made Vietnam very weak in comparison with the world in using one of the best renewable and clean energy, solar energy.

At the Laboratory for Nanotechnology (LNT), several solar cell projects has been awarded to perform early research in order to create high efficiency monocrystalline solar cells, and to prepare for the future research on low cost solar cells. This report describes works about the process improvement of short circuit current (J_{SC}) to increase cell efficiency.

The solar efficiency is determined by the following formula [1]:

$$\eta = \frac{V_{OC} J_{SC} FF}{P_{in}} \quad (1)$$

Where η is the cell efficiency; FF is the fill factor; P_{in} in the incoming light intensity.

According to the above formula, high efficiency cell can only be obtained by increasing FF, J_{SC} and V_{OC}. The fill factor is the first parameter needed to be improved because it determines the maximum power from a solar cell and can be enhanced through

the front contact optimization, which affects the contact resistivity and the shadow loss and thus increase the free carrier collection ability. Meanwhile, getting a good V_{oc} needs very complex processes but getting a good J_{SC} is simpler. Therefore in order to create high efficiency solar cells, the short circuit current needs to be considered carefully.

The short circuit current is determined by the generation and the collection of photo-generated carriers. The carrier generation depends mainly on the cell front and rear reflectance and the collection depends on the cell resistances and front, edge, rear and bulk recombination. A large amount of short circuit current can only be obtained when minimizing the cell reflectance and the cell recombination. All of these factors that drop down the short circuit current is shown in Fig.1 [2].

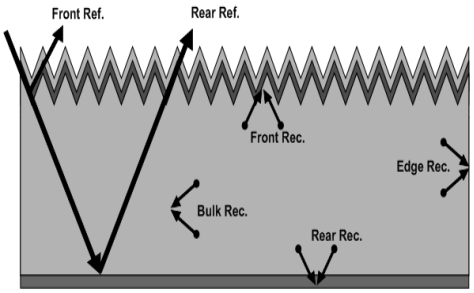

Figure 1. Short circuit current consumption

In this report, we only investigated the loss of short circuit current on the front surface of monocrystalline solar cell. Firstly, the optimization of front contact was used to enhance the cell's fill factor and the carrier collection. Then, two methods were used to improve cell's light absorption ability: (i) surface treatments using tetramethyl ammonium hydroxide (TMAH, $(CH_3)_4NOH$) solution to create random pyramids surface and (ii) deposition of anti-reflection coatings (titan silicate TiO_2/SiO_2 or indium tin oxideITO or silicon nitride SiN_x layers) for further reducing the reflectance. Besides, SiN_x layer also plays the role of passivating surface dangling bonds. It was shown that hydrogen released from the SiN_x layer fabricated by PECVD method can passivate silicon defects[3,4]. In fact, the passivation ability of ITO layer is not as good as SiN_x layer, but it plays the role of the extra contact due to its good conduction, thus still allowing the better carrier collection. The J_{SC} improvement diagram in our study is shown in Fig.2.

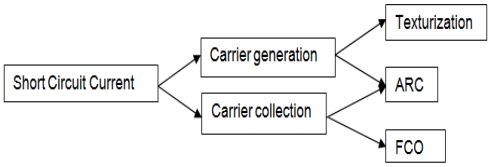

Figure 2. The improvement diagram of Short Circuit Current can be carried out in two methods (i) increasing the carrier generation and (ii) enhancing the carrier collection. ARC – anti reflection coating; FCO – font contact optimization

The other losses of short circuit current in the solar cell are due to the cell reflectance and the surface recombination at rear and edge of the solar cell, which have not been examined yet in this study because of its complexity and correlations.

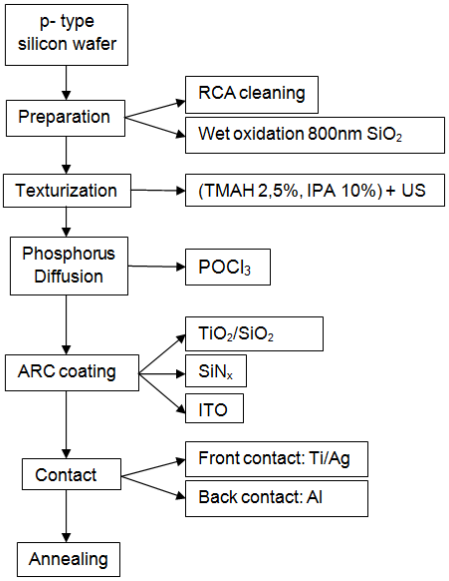

Figure 3. The solar cell fabrication process at LNT

2. EXPRIMENTAL DETAILS

Mono crystalline silicon solar cell was made from semiconductor-grade silicon (SeG-Si) 4 inch wafer, with the crystal orientation of <100>; p-doped and the resistivity of 1-10 Ωcm; one side polished. With the purity of 99,999999999 %, this type of silicon has very little lattice defects so the carrier collection losses inside the solar cell can be considered small, and this permits to get the short circuit current solar cells.

In this work, six types of mono crystalline solar cell were investigated to improve the short circuit current, except the first sample that only had the phosphorus diffusion and not-optimized front contact, the other had more optimization.

Table 1. Cells' conditions

Sample	Texturization	Diffusion	Anti-Reflection Coating	Front Contact Optimization	Annealing
3273	-	X	-	-	X
1067	-	X	-	X	X
5188	X	X	-	X	X
6060	X	X	TiO_2/SiO_2	X	X
1016	X	X	SiN_x	X	X
2217	X	X	ITO	X	X

Phosphorus was diffused into the front surface by phosphoryl chloride $POCl_3$ in diffusion furnace at 850°C. Titanium and silver layers (20nmTi/600nmAg) is evaporated by electron beam system to create front contacts. Meanwhile, aluminum layers (1µm Al) issputtered for depositing full wafer back contacts.

The front contact grid was optimized according to [5], by using the following formula:

$$nw_1 = J_L ac \sqrt{\frac{\rho_f}{3P_L \eta_1 t}} \qquad (2)$$

Where n: numbers of finger; w_1 :finger width; J_L : light-generated current, a and c : based on cell dimension;

ρ_f : metal resistivity; P_L : light intensity, η_1 : cell efficiency, t : contact thickness

For reducing the surface reflectance, texturization process used TMAH solution (TMAH 2,5%; IPA 10%), enhanced by ultrasonic in 20 minutes to create random pyramids structure on the solar cell surface[6],[7]. The anti-reflection coating layers were deposited for having better reflectance reduction: titanium silicate layer (TiO_2/SiO_2) is fabricated by spin coating method, while ITO layer by the sputtering method [8] and SiN_x layer by the PECVD method [9].

The solar cells' efficiency was measured under off-standard 21m W/cm2 irradiation intensity of arc xenon lamp. Then all cell parameters are fitted with IV-Fit program of Energy research Centre of the Netherlands by using the two-diode model

$$J = J_{01}\left[\exp\left(\frac{e(V-JR_s)}{kT}\right)-1\right]+J_{02}\left\{\exp\left(\frac{e(V-JR_s)}{2kT}\right)-1\right\}+J_{lt}+\frac{V-JR_s}{R_{SH}} \quad (3)$$

and the orthogonal distance regression method [10] to double check the cell parameters in comparison with the values given by the solar simulator SS150 (Photo Emission Co.) and to find out the cell series resistance RS and the cell shunt resistance RSH.

3. RESULTS AND DISCUSSION

All measured parameters are presented on the Table 2 and corresponding fitted parameters are shown on the Table 3.

Table 2. Measured cell parameters

Cell ID	Voc (mV)	J_{SC} (mA/cm^2)	FF(%)	η(%)
3273	535	5.21	43	5.76
1067	519	5.37	72	9.60
5188	531	4.93	33	4.14
6060	514	5.83	69	9.98
1016	526	7.61	68	13.14
2217	527	7.92	64	12.81

Table 3. Fitted cell parameters

Cell ID	V_{OC} (mV)	J_{SC} (mA/cm2)	R_S (Ω)	R_{SH} (Ω)	η (%)	J_{lt} (A/cm2)	J_{01} (A/cm2)	J_{02} (A/cm2)
3273	533	5.4	2.7	185	5.76	5.5E-3	4.5E-14	8.4E-8
1067	520	5.3	3.5	∞	9.66	5.3E-3	5.7E-12	9.1E-8
5188	531	5.06	50.6	113	4.14	7.3E-3	9.3E-14	8.9E-8
6060	515	5.9	5	2082	9.98	5.9E-3	7.2E-12	1.1E-7
1016	527	7.6	6.5	74783	13.14	7.8E-3	2.3E-12	2.2E-7
2217	528	7.8	6.2	∞	12.81	7.6E-3	4.2E-12	1.7E-7

Our first sample, the cell ID 3273 is the simplest one with only the phosphorus diffusion in polished silicon surface and not-optimized front contact grid structure. Its short circuit current was only 5.21 mA/cm^2 and 43% of fill factor. The low short circuit current and fill factor are probably due to:

1. the shunt resistance (R_{SH})istoo low, thus dumps the fill factor and the carrier collection ability,
2. the cell surface reflectance is too high (40% of weight-averaged reflectance) which causes poor carrier generations, and
3. silicon surface are not passivated, so the surface recombination is quite high so reducing the carrier collection ability[11].

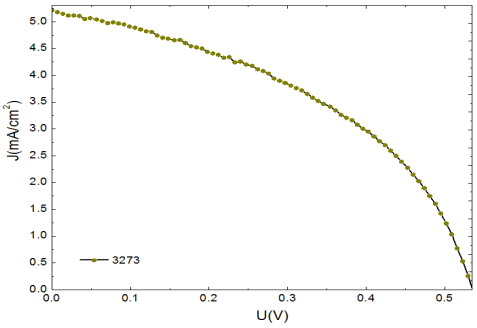

Figure 4. JV curves of cell ID 3273, the simplest cell with bad cell resistances and the high front surface reflectance and front surface recombination

The front contact optimization has been carried out to obtain highershunt resistance with the sample ID 1067. As the results, the fill factor increased significantly from 43% to 72%. Due to the increase of the FF, the efficiency raised up to 9.66%. Still, the short circuit current was low, because the low light absorption and low carrier collection possibility was not solved yet.

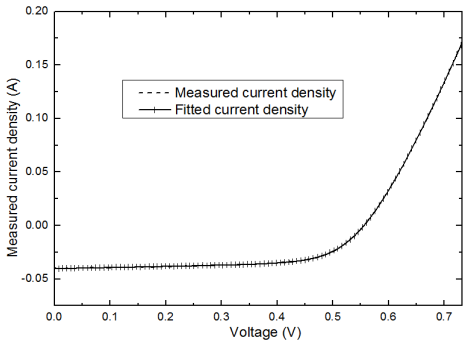

Figure 5. JV curves of the cell ID 2217 (the fitting curve with symbols using orthogonal distance regression method). The small deviation between fitted and measured curve proves the reliability of extracted parameters.

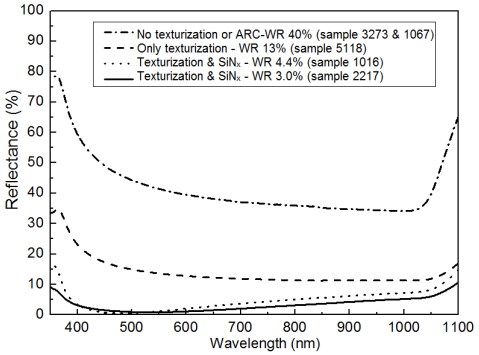

Figure 6. Influence of texturization and ARC on the reflectance spectra

In the sample ID 5188, in order to reduce the high reflectance surface, anisotropic etching in TMAH solution was performed. This creates random pyramids on the silicon surface, which decreases dramatically the total reflectance (down to 13% from 40% of polished surface). This makes sample 5188 possessing the good light absorption property. But the pyramids surface of sample 5188 has a larger surface area than the flat surface of sample 3273 or sample 1067. Thus the number of dangling bonds on the silicon surface of sample 5188 is greater and cause the carrier collectionpossibility drops down due to the high surface recombination. As the results, the short circuit current was decreased to 4.93 mA/cm^2.

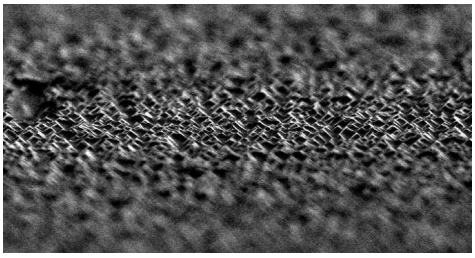

Figure 7. SEM image of random pyramids structure after the TMAH surface treatment

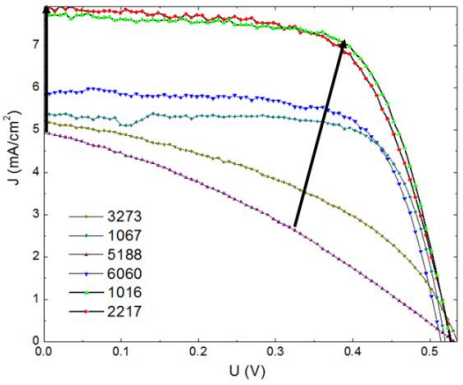

Figure 8. The short circuit improvement; 1016 (SiN_x) and 2217(ITO) are the best cells due to their best short circuit currents. All measures were under 21 mW/cm^2 of irradiation.

Three types of anti-reflection coating (TiO_2/SiO_2, SiN_x and ITO) were used on the random pyramids structure for the passivation of dangling bonds on silicon surface. More importantly, the anti-reflection coating also reduce the surface reflectance: the SiN_x sample (ID 1016) had 4.4% of reflectance and the ITO sample (ID 2217) had about 3% of reflectance. In consequence, the short circuit current of the

TiO_2/SiO_2 spin coated cell (ID 6060) increases to 5.9 mA/cm^2. In the SiN_x layer, with a large amount of free hydrogen radical originating from plasma gas dissociation, is the best passivation layer. Hence, the SiN_x sample had better J_{SC} : 7.6mA/cm^2. The ITO layer play less role in passivating dangling bonds than SiN_x layer, but it plays more role of an extra contact due to its conduction and thus had a better reflectance, giving better carrier collections and the best J_{SC}: 7.8mA/cm^2.

The short circuit improvement affects cell efficiency, displays in the JV curves improvement (Fig 8). The cell ID 1016 (SiN_x) and ID 2217 (ITO) curves are the best JV curves due to their best short circuit current: 7.6 mA/cm^2 and 7.8 mA/cm^2. One also can see that the open circuit voltage fluctuate slightly from one to other cells even the back contact deposition method is the same.

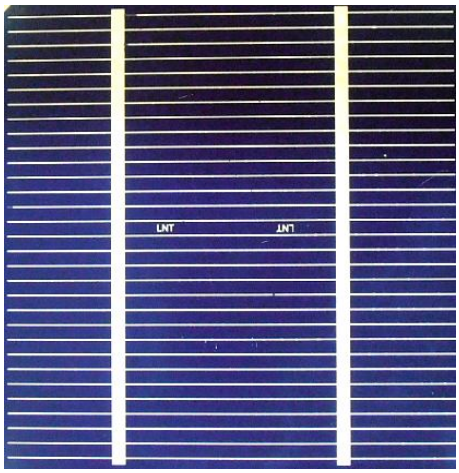

Figure 9. 2217 Solar cell, with front contact optimization, texturization and ITO antireflection coating ; η = 12.81%

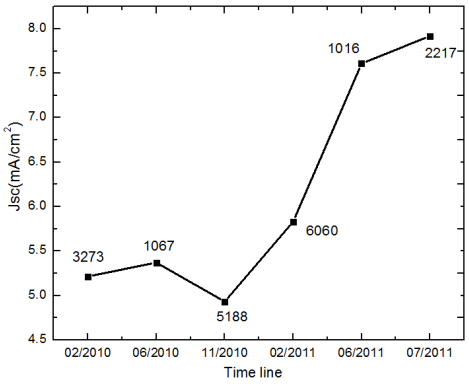

Figure 10. Short circuit current improvement; 2217 sample with ITO coating has the best J_{SC}

In the figure 9, we show the image taken on the front side of the solar cell ID 2217. Two bus bar structure and fingers with the symbol of LNT can be easily seen on the surface. In the figure 10, we show the evolution of J_{sc} improvement by adding and using step by step more efficient processing method.

4. CONCLUSION

Three methods to improve the short circuit current at front surface were showed: (i) front contact optimization to reduce cell resistances, (ii) surface treatment with TMAH solution and (ii) anti-reflection coating to enhance light absorption. However, surface treatment increases surface recombination, thus reducing J_{SC} (cell ID 5188: 5.06 mA/cm^2) and requiring anti-reflection coating to passivate the dangling bonds. Finally, all three ARC samples showed a good passivation ability and made J_{SC} higher than non texturized sample (ID 1067: 5.37 mA/cm^2). From the cell ID 3273, with J_{SC} about 5.2 mA/cm^2, which was not optimized, to the last one (ITO and SiNx), which had enough

optimization on the front, the short circuit current has been greatly enhanced to the value of 7.8 mA/cm^2, 150% of increasing;. As the results, the cell efficiency increased from 5.76% to 12.81%, showing the reliability of our methods in improving short circuit current. However, the open circuit voltage is nearly the same (535mV and 527mV), which may need to be examined in future research to increase more the cell efficiency.

CẢI THIỆN DÒNG NGẮN MẠCH TRONG PIN MẶT TRỜI SILIC ĐƠN TINH THỂ

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TÓM TẮT: *Trong bài báo này chúng tôi trình bày chuỗi các thí nghiệm nhằm từng bước cải thiện dòng ngắn mạch trong pin mặt trời silic đơn tinh thể, từ đó gia tăng hiệu suất của pin. Thứ nhất, chúng tôi tối ưu hóa lớp điện cực mặt trước để giảm thiểu sự che sáng do điện cực và điện trở của pin. Thứ hai, chúng tôi nghiên cứu các phương pháp xử lý bề mặt đế silic để tạo ra bề mặt nhám nhằm giảm độ phản xạ toàn phần và làm tăng khả năng hấp thụ ánh sáng của đế silic. Cuối cùng chúng tôi nghiên cứu hai loại màng chống phản xạ khác nhau cho pin mặt trời: màng silicon nitride với khả năng thụ động hóa bề mặt và màng indium tin oxide với khả năng dẫn điện để giảm hơn nữa độ phản xạ toàn phần trên đế silic. Kết quả thu được pin mặt trời có hiệu suất 13%, với thế hở mạch 527mV, hệ số điền đầy 68% và dòng ngắn mạch vào khoảng 7.92 mA/cm^2 dưới cường độ ánh sáng tới 21mW/cm^2.*

Từ khóa: *pin mặt trời đơn tinh thể, điện cực mặt trước, phương pháp xử lý bề mặt, lớp chống phản xạ.*

REFERENCES

[1]. Adolf Goetzberger, Joachim Knobloch, Bernhard VoB, *Crystalline Silicon Solar Cells, by John Wiley & Sons Ltd*, 69-72 (1998).

[2]. William P. Mulligan, Doug H. Rose, Michael J. Cudzinovic, Denis M. De Ceuster,Keith R. McIntosh, David D. Smith, and Richard M. Swanson, Sun Power Corporation, *Manufacture of Solar Cells With 21% Efficiency* (June 2004).

[3]. Rohatgi A., Yelundur V., Jeong J, Ebong A., Meier D., Babor A. M., Rosenblum M. D., *Proc.16th European Photovoltaic Solar Energy Conf.*, Glasgow, 1120 (2000).

[4]. Winderbaum S., Cuevas A., Chen F., Tan J., Hanton K., Macdonald D., Roth K.,

Proc. 19th European Photov. Solar Energy Conf., Paris, 576 (2004).

[5]. Hoang Ngoc Vu, Tong Duy Hien, Duong Dinh Hiep, Dang Mau Chien, Nguyen Tran Thuat, Study And Optimization Of Front Contact For Solar Cell, *The 5th International Workshop on Advanced Materials Science and Nanotechnology* (IWAMSN2010) - Hanoi, Vietnam, MEP-P11 (2010).

[6]. P. Papet, O. Nichiporuk, A. Kaminski, Y. Rozier, J. Kraiem, J.-F. Lelievre, A. Chaumartin, A. Fave, M. Lemiti, Pyramidal texturing of silicon solar cell with TMAH chemical anisotropic etching, *Solar Energy Materials and Solar Cells*, ISSN: 09270248, Vol:90, Issue: 15, 22, 2319-2328 (September 2006).

[7]. Le Nguyen Ngan, Hoang Ngoc Vu, Tran Ngoc Linh, Dang Mau Chien and Nguyen Tran Thuat,Study of texturizing and etching of monocrystalline silicon and effect of SiN_x, ITO ARC for solar cell Applications, *The 12th Conference On Science and Technology*, University of Technology – VNU HCM (submitted) (26 - 28/10/2011).

[8]. Le Thanh Hung, Hoang Ngoc Vu, Dang Mau Chien, Nguyen Tran Thuat, Deposition Of ITO Thin Films Used As Top Electrode And Antireflection Layers Of Silicon Solar Cell By Magnetron Sputtering, *The 12th Conference On Science and Technology*, University of Technology – VNU HCM (submitted) (26 - 28/10/2011).

[9]. Le Tran Hoang Long, Dang Mau Chien, Nguyen Tran Thuat,Study Of Deposition Of SiN_x Thin Film By PECVD Used As Anti-Reflection Coating And Surface Passivation Layer In Solar Cell, *The 12th Conference On Science and Technology*, University of Technology - VNU HCM (submitted) (26 - 28/10/2011).

[10]. A.R. Burgers J.A. Eikelboom A. Schönecker W.C. Sinke, Improved Treatment Of The Strongly Varying Slope In Fitting Solar Cell I-V Curves, *Photovoltaic Specialists Conference*, Conference Record of Twenty Fifth IEEE 13-17, 569-572 (May 1996).

[11]. T. Lauinger, J. Schmidt, A. G. Aberle, R. Hezel, *Appl. Phys. Lett. 68*, 115936 (1996).