Designing an uninterruptible power supply based on the high efficiency push–pull converter

- **Le Minh Phuong**
- **Phan Quoc Dzung**
- **Nguyen Minh Huy**
- **Nguyen Hoai Phong**

University of Technology,VNU-HCM

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ABSTRACT:

This paper presents an implementation of the DC/DC push–pull converter for an uninterruptible power supply (UPS). Some classical DC/DC converters are presented and analyzed for pointing out their advantages and drawbacks. Besides, an original system based on a push-pull converter associated with a dynamic modulation control is chosen. The main advantage is ~~the~~ possibility to control the delivered electric power in a wide range from very low level to high level of voltage within the same basic architecture. It can reduce the switching power losses and increase the power conversion efficiency. This paper proposed a new control scheme of the DC/DC converter and DC/AC inverter. The suggested system consists of a high efficiency DC/DC converter and a single-phase DC/AC inverter has been simulated using Matlab/Simulink and designed basing on the DSP TMS320F28027. Both results show high performances of the DC link and AC load voltages, when load changes from zero to rated. The performance of the proposed system has been verified through a 1kW prototype of the system for a 50 Hz/220-230 VAC load sourcing by two series connected batteries of 12V. The proposed DC/DC converter achieves a high efficiency of 93.0%. The system including the DC/DC converter and DC/AC inverter achieves an efficiency of 91.2% and Total Harmonic Distortion (THD) of AC load voltage reached 1.9%.

Key words: *DC/DC converter, push–pull converter, uninterruptible power supplies (UPS), inverter.*

1. INTRODUCTION

An uninterruptible power supply is an electronic device that provides an alternative electric power supply to connect electronic equipment when the primary power source is not available. The UPS systems provide ~~for~~ a large number of applications in a variety of industries.

Conventional UPSs, which are shown in Figure 1, have very low efficiency, about 70-80%. Because of the topology consists of AC transformer, its power loss is very high. Moreover, semiconductors of the DC/AC inverter work with high current, leading power loss decreases. Some new UPSs have efficiency of 87% - [1].

To correct disadvantages of conventional UPS and increase their efficiency, the paper proposed a new topology of UPS, a block scheme is shown in Figure 2.

In the new proposed topology, in UPS applications, they need dischargers to draw power from batteries. The voltage level of batteries is much lower than that of DC-Link bus; and in order to generate 50 Hz, 220-230Vac. Thus, a converter with a high step-up voltage ratio is required for the dischargers. Furthermore, to effectively utilize the energy stored in batteries, the dischargers should be designed with high efficiency and the output voltage of the DC/DC converter should be high enough to generate the DC-link voltage [1], [2],[3]. Up to now, various DC/DC converters have been investigated for high step-up applications. These DC/DC converters are divided into five basic topologies: Fly-back Converter, Forward Converter, Half-Bridge Converter, Full-Bridge Converter and Push-Pull Converter [2][3]. After analysis advances and drawbacks of these converters, a push-pull DC/DC converter has been chosen.

In this paper, a push–pull converter for UPS applications is proposed. The proposed converter is depicted ina DC-link voltage controller is described for a constant DC-link voltage regulation. A digital model has been designed on DSP TMS320F28027, and prototype 1kW with a 50 Hz/220 Vac has been implemented. Experimental results show that ripple of Dc link is less than 1.5%, total efficiency is 91.2%.

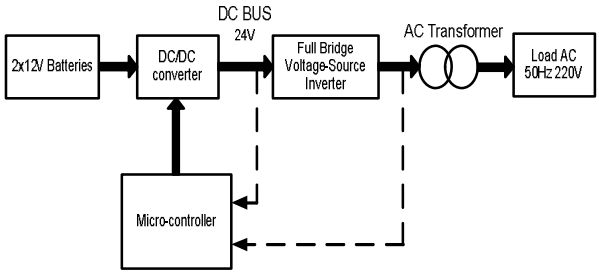


Figure 1. Conventional UPS topology

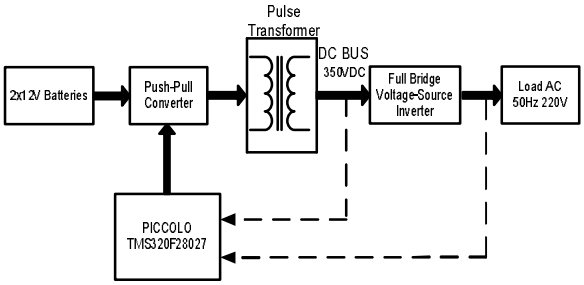


Figure 2. Proposed UPS topology

2. ANALYSIS OF DC/DC TOPOLOGIES

Because the output voltage of the DC/DC converter should be high enough to generate the DC-link voltage around 350 V, and battery has a low voltage ranges from 20 V to 24 V, so a DC/DC converter has been investigated for high step-up applications. For this application, below DC/DC converters are chosen. These DC/DC converters provide an electrical isolation between the input and output of the converter. Selection of a topology depends on careful analysis of the design specifications, cost and size requirements of the converter. Operation of each of the above topologies is described in the following sections of this application note. Details of the topology selection and hardware design are provided in below sections.[4],[5]

2.1. Forward Converter

A forward converter, which can be a step-up or step-down converter, is shown in Figure 3(a). When the transistor Q is ON, VIN appears across the primary, and then generates output voltage determined by equation 1. The diode D1 on the secondary ensures that only positive voltages are applied to the output circuit while D2 provides a circulating path for inductor current if the transformer voltage is zero or negative. A third winding is added to the transformer of a forward converter, also known as a "reset winding". This winding ensures that the magnetization of the transformer core is reset to zero at the start of the switch conduction. This winding prevents saturation of the transformer.

$$V_{out} = DV_{in}\frac{N_2}{N_1} \qquad (1)$$

Where: D is the duty cycle of the transistor Q and N_2/N_1 is the secondary –to-primary turns ratio of the transformer

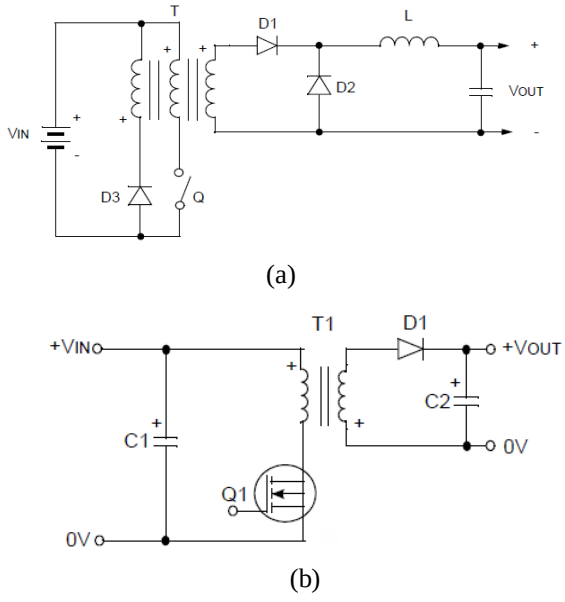


Figure 3. A DC/DC Forward converter (a); And DC/DC Fly-back converter (b)

One problem with the Forward topology is that the primary switch voltage can rise essentially unconstrained. When the switch turns off, energy stored in the transformer primary wants to cause current to continue to flow toward the FET drain. And resetting of a transformer is a

cause to limit the maximum duty cycle that a Forward converter can operate. These issues tend to limit the power level, that a Forward converter is best used for power levels between 30W and 150W [1],[2]. Moreover, Forward Converter hashigh input ripple current. So it tends to decrease a quality of output voltage and current

2.2. Fly-back Converter

Figure 3(b) shows a fly-back converter circuit. When transistor Q1 is ON, due to the winding polarities, the diode D1 becomes reverse-biased. Therefore, transformer core flux increases linearly. When transistor Q1 is turned OFF, energy stored in the core causes the current to flow in the secondary winding through the diode D1 and flux decreases linearly. Output voltage is given by

$$V_{out} = \frac{D}{1-D} V_{in} \frac{N_2}{N_1} \qquad \textbf{(2)}$$

The fly-back converter suffers from high power losses due to its hard-switching operation. Especially, for the high step-up applications like battery, the hard-switching operation causes high power losses. Considering its operating conditions for the harshest environment, the life time of the UPS system is reduced [1],[2],[3].

2.3. Half-Bridge Converter

Figure 4(a) shows the half-bridge converter. In this converter, the reversal of the magnetic field is achieved by reversing the direction of the primary winding current flow. In this case, two capacitors C1 and C2 are required to form the DC input mid-point. Transistors Q1 and Q2 are turned ON alternately to avoid a supply short circuit, in which case the duty cycle, d, must be less than 0.5. For the half-bridge converter, the output voltage VOUT equals that of equation 3.

$$V_{out} = DV_{in} \frac{N_2}{N_1} \quad (3)$$

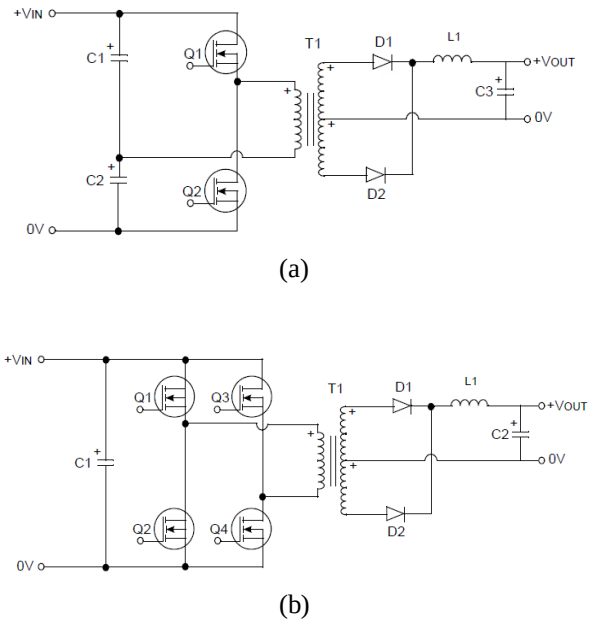


Figure 4. A DC/DC Half-Bridge converter (a) and DC/DC Full-Bridge converter (b)

The half-bridge topology has some disadvantages: it features a split capacitor bus, twice the device current and twice transformer turn ratio, leading to increased transformer loss and size. The Half-Bridge DC/DC Converters have efficiency lower than the other one during a light load. They are working at half the supply voltage the switching transistors are working at twice the collector current compared with the basic push pull circuit. [1],[2],[3].

The asymmetrical half-bridge fly-back converter has been utilized to reduce the switching power losses for low voltage DC source. It reduces the switching power losses by the soft-switching operation for the switching power devices [8],[9]. The half-bridge fly-back converter in [8], however, requires a large turns ratio of the transformer for generating a high DC-link voltage from the low voltage batteries. The large transformer turns ratio causes high voltage stresses on the switching power devices.

2.4. Full-Bridge Converter

The full-bridge converter topology is shown in Figure 4 (b), is basically the same as the half-bridge converter, where four transistors are used. Diagonal pairs of transistors (Q1-Q4 or Q2-Q3) conduct alternately, thus achieving current reversal in the transformer primary. Output voltage equals that of equation 4.

$$V_{out} = 2DV_{in}\frac{N_2}{N_1} \quad (4)$$

The full-bridge topology is well suited for applications that require a wide input voltage range. The full-bridge converter with a phase-shift control has been used for high step-up applications. However, the phase shifted full-bridge converters [10,11] require lots of power switching devices and the associated control circuits. So, the manufacturing cost of the system increases, which limit the practical utilization of the UPS system.

To optimize the global efficiency of the boost converters based on classical inverters described above, we designed a converter with a symmetric architecture using push-pull structure. The Push-Pull converters have several advantage characteristics in comparison of other topologies. A Push-Pull Converter is converter with a bi-directionally driven isolation transformer. Push-Pull transformers and filters are much smaller than others. A Push-Pull Converter has a low output ripple current, a lower input ripple current, and a simple gate drive. Moreover, the better core utilization and the lack of a realistic duty cycle limit in the Push-Pull architecture allows them to operate at significantly higher power levels. For moderate input voltages Push-Pull converters are useful to 500W and beyond [1],[2],[3].

3. THE OPERATION OF THE PROPOSED PUSH–PULL CONVERTER

The Figure 5 represents the electronic schema of the proposed boost voltage converter using the push pull structure. We can clearly observe in this schema the symmetrical structure of the output stage. Within this configuration, the transformer works in a forward mode at high frequency 20 kHz, and, thus, it allows the possibilities to minimize the coupled coils element even in case of conversion of high power. Moreover, the symmetrical structure of the push-pull stage allows the use of the two quadrants of the magnetic cycle of the transformer, the main advantage being the size optimization of the coils.

The operation of push-pull converter: When Q1 switches ON, current flows through the upper half of the T1 transformer primary and the magnetic field in T1 expands. The expanding magnetic field in T1 induces a voltage across the T1 secondary; the polarity is such that D2 is forward-biased and D1 is reverse-biased. D2 conducts and charges the output capacitor C2 via

L1. L1 and C2 form an LC filter network. When Q1 turns OFF, the magnetic field in T1 collapses and after a period of dead time (dependent on the duty cycle of the PWM drive signal), Q2 conducts, current flows through the lower half of T1's primary, and the magnetic field in T1expands. At this point, the direction of the magnetic flux is opposite to that produced when Q1 conducted. The expanding magnetic field induces a voltage across the T1 secondary; the polarity is such that D1 is forward- biased and D2 is reverse-biased. D1 conducts and charges the output capacitor C2 via L1. After a period of dead time, Q1 conducts and the cycle repeats.

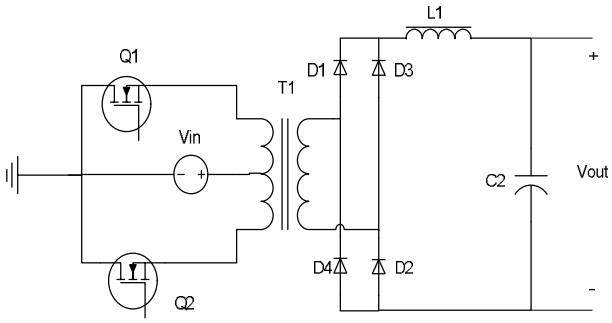


Figure 5. Proposed DC/DC Push-pull converter

There are two important considerations with the push-pull converter:

• Both transistors must not conduct together, as this would effectively short circuit the supply. This means that the conduction time of each transistor must not exceed half of the total period (D < 0.5) for one complete cycle, otherwise conduction will overlap.

• The magnetic behavior of the circuit must be uniform; otherwise, the transformer may saturate, and this would cause destruction of Q1 and Q2. This behavior requires that the individual conduction times of Q1 and Q2 must be exactly equal and the two halves of the center-tapped transformer primary must be magnetically identical. These criteria must be satisfied by the control and drive circuit and the transformer. The output voltage equals that of Equation 5.

$$V_{out} = 2DV_{in}\frac{N_2}{N_1} \quad (5)$$

Where: D is the duty cycle of the transistor Q1 and Q2 $0<D<0.5$

3.1. Push-Pull Switching Waveforms

Figure 6 shows oscilloscope waveforms for the drain voltages of the two primary switches and the output inductor current. When neither switch is active then both drain voltages are at the input voltage potential. It can be seen in the figure that there can be significant overshoots beyond the expected 2·Vin.

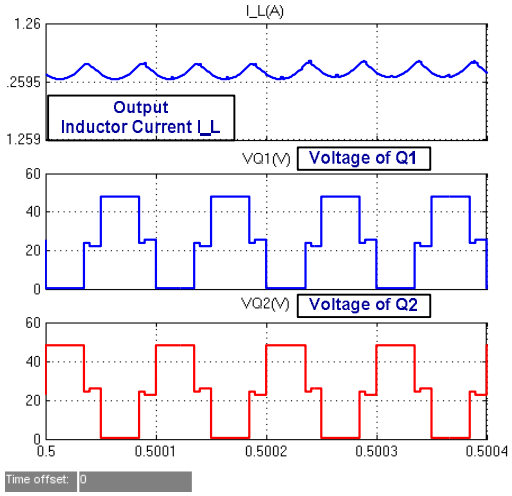


Figure 6. Waveform of MOSFET voltage

4. PROPOSED CONTROL SCHEMES

To achieve a high quality of load voltage and current (a rate amplitude and low THD), two control schemes have been developed. The first one allows keeping DC-link constant and the second one allows keeping AC voltage, current under rate parameters.

4.1. Push-Pull Control Loop

The push-pull converter is controlled with a voltage mode control scheme. The PWM module is configured for Push-Pull mode with an independent time-base. The DC Link voltage is measured by the voltage sensors and sent to DSP control. This value is subtracted from the voltage reference in software to obtain the voltage error. The voltage error is then fed into a control algorithm that produces a duty cycle value based on the voltage error, previous error, and control history. The output of the control algorithm is also clamped to minimum and maximum duty cycle values for hardware protection. The voltage mode control algorithm must be executed at a fast rate in order to achieve the best transient response. Therefore, the control algorithm is executed in the ADC interrupt service routine, which is also assigned the highest priority in the UPS code. A block diagram of the push-pull converter control scheme is shown in Figure 7.

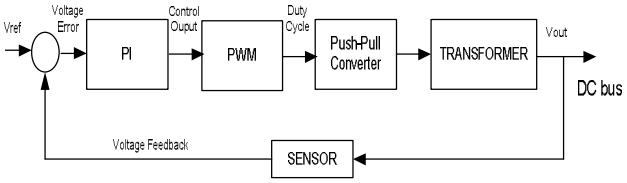


Figure 7. A Block diagram of Push-pull voltage control loop

4.2. Inverter Control Loop

The inverter output is generated by varying the voltage reference using a sinusoidal PWM. The measured output voltage is subtracted from the present reference value and the voltage error is obtained. The voltage error is fed into the voltage error compensation algorithm. The output of the voltage error compensator produces the current reference value. The measured output current is subtracted from the current reference to obtain the current error. The current error is used as the input to the current error compensation algorithm to produce the command signal for the PWM module. The result of the control loop is added to the nominal duty cycle for one leg of the full-bridge inverter and subtracted from the nominal duty cycle for the second leg. A block diagram of the full-bridge inverter control system is shown in Figure 8.

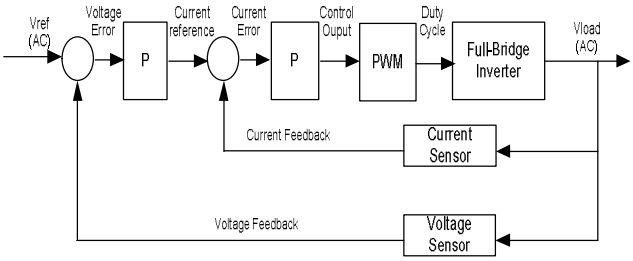


Figure 8. A Block diagram of the full-bridge inverter control system

5. SIMULATION OF THE PROPOSED CONTROL SCHEME

The proposed control scheme has been simulated by Matlab/Simulink software and presented in Figure 9. In the scheme, the battery presented as an ideal DC power source voltage is 24V. Semiconductor components in the Push-Pull are MOSFETs. The transformer is isolated and has a transformer ratio 1:18. Semiconductor components of the DC/AC inverter are IGBT, and AC load is static load under rated power 1000W. The coefficient Kp, Ki in the control block is defined experimentally during a simulation process. It should be noted, the load current peak value has not been exceed rated, so saturation block must be in the current control block circuit DC/AC. Moreover, LC filter with the following L=2mHC=3.3uF is used to achieve true sin AC voltage output of the inverter.

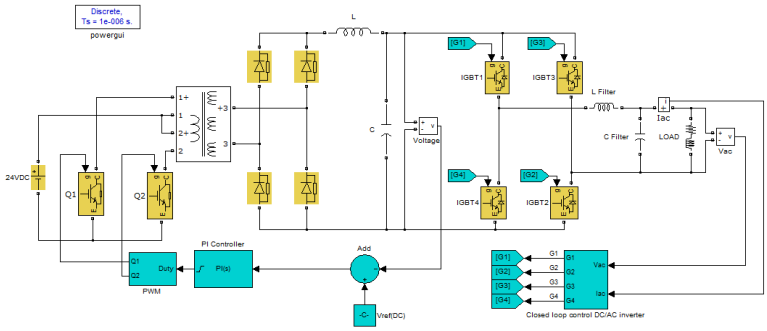


Figure 9. Simulation model of proposed push-pull topology

The simulations have been done for modes with load changes, as follows

Case study 1: The models started with 1/3 rated load to moment t= 0.2s. During the interval 0.2s-0.4s load is 2/3 rated load and during the interval 0.4s-0.6s load is the norm. Simulation results are presented in Figure 10(a), which shows that at the moment 0.2s and 0.4s load is changed, but DC-link voltage and voltage were almost constant.

Case study 2:Themodelis started with a rated load. At 0.2sloadisreducedtonearly zero. Simulation resultsare presentedin Figure 10(b). In the figure, when the load is rated DC-link voltage is 335V, and while load is near zero DC link voltage is upto341V. The voltage isestablishedatthemomentof0.8s, and the response time is 0.6s.

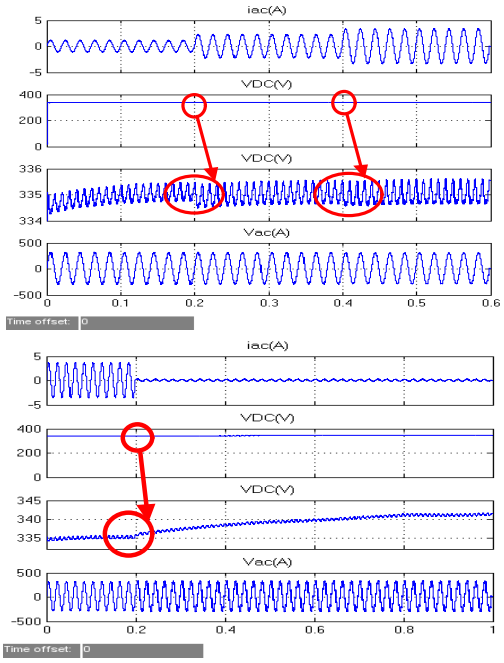


Figure 10. The wavefrom of current load, DC link and load voltage: for case study 1(a), case study 2(b)

5. THE DESIGN PROTOTYPE AND EXPERIMENTAL RESULTS

To illustrate the [analysis] and discussion, a 1kW prototype with proposed topology has been built. The schematic diagram of the proposed converter is depicted in Figure.2. The new control algorithm is programmed in the control board **DSP TMS320F28027** to generate the command pulses for DC/DC push-pull converter and DC/AC full bridge inverter. The central processor unit of proposed converter is TMS320F28027. This is a 32 bit DSP controller of Piccolo family of Texas Instrument. F28027 has 2 Enhanced Pulse Width Modulator (ePWM) which have 12 PWM output compatible for 1 phase and 3 phase inverter.

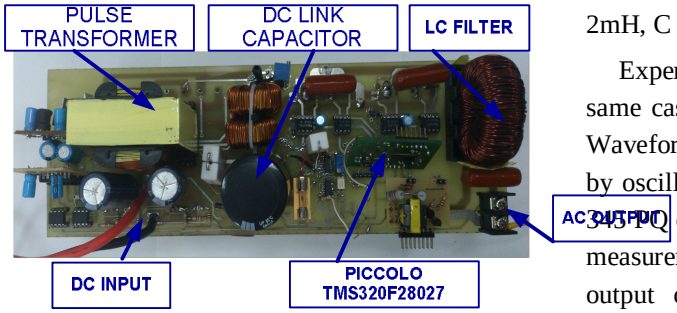


Figure 11. The experimental prototype

The prototype divides in 2 parts: DC/DC converter and DC/AC inverter. DC/DC is a step up converter using push pull configuration switching at 20KHz. Input voltage can be vary from 20 to 24V DC. High voltage DC bus is regulated at 330-350VDC which used to generate a 50Hz, 200Vrms output true sin by a sinusoidal H-Bridge DC/AC PWM inverter. The efficiency of system is 91.2% at full load. The experimental prototype is shown in Figure.11.

5.1. Push-pull converter specifications

Input and output voltages: 20 – 26VDC, 330VAC

Output power: 1KW

DC Input capacities: 4700uF/35V .DC Output capacity: 680uF/400V

DC primary Switch: 2 Fets IRFB4110 in parallel.

Secondary bridge rectifier diodes: STTH2006

Pulse transformer: EE55 core, NP1 = NP2 = 3 turns, NS = 54 turns.

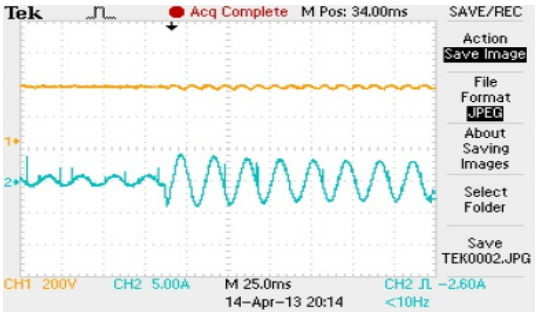
Primary inductance: L1 = L2 = 70uH, Primary leakage inductance: $L_{LK1} = L_{LK2} = 3uH$.

5.2. DC/AC sinusoidal h-bridge inverter specifications

H-Bridge uses 4 IGBT 30N60 controlled by Piccolo TMS320F28027 switching at 20kHz. The LC filter is designed for low THD, with L = 2mH, C = 3.3uF, THD is established at 2%.

Experimental results have been got by the same cases studies as in the simulation process. Waveforms of voltages and current are measured by oscilloscope Tektronix TDS2024B and Fluke 345PQ clamp meter. Figure 12, Figure.13 shows measurements of DC link voltage, output voltage, output current under input voltage and load variations, from which it can be observed that tight regulation can be achieved.

Case study 1: Themodelsstartedwith 1/4 rated load and at moment t=0.2s load up to a rated.



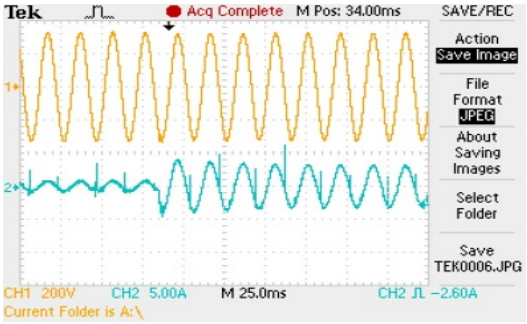
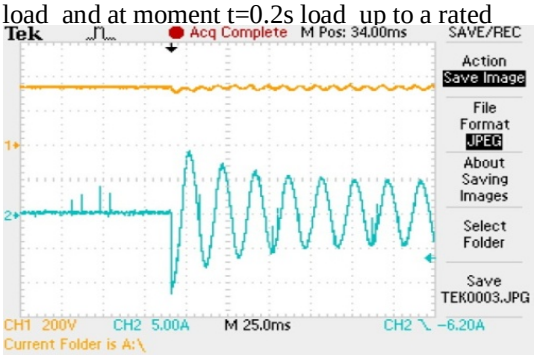


Figure 12. Experimental waveforms :DC link voltage, output voltage and output current

Case study 2:Themodelis started without a load and at moment t=0.2s load up to a rated



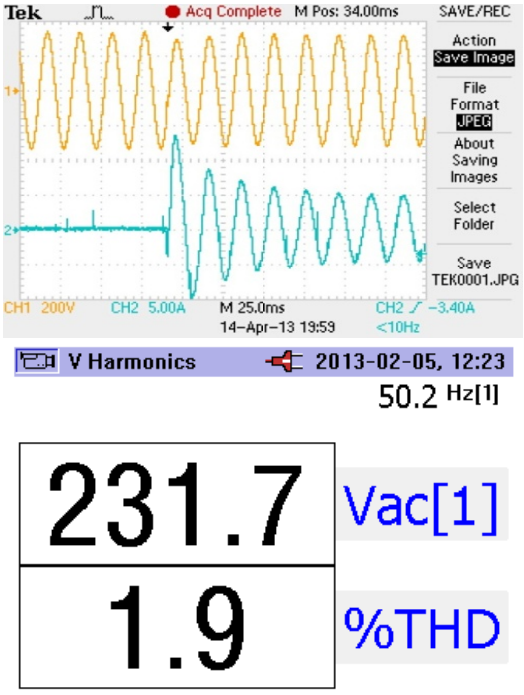


Figure 13. Experimental waveforms: DC link voltage, output voltage and output current and a spectrum of AC output voltage

Measured results of power efficiency of UPS using proposed push–pull converters are listed in Tables 1.

Table 1. Power efficiency of UPS

P_{in}(W)	V_{in} (V)	I_{in}(A)	P_o(W)	η (%)
146	24.6	14.6	117	78.2
275	24.3	27.6	238	85.5
403	24	34.5	352	87.3
646	23.6	44.4	575	89.0
886	23.2	52.3	801	90.3
1125	22.8	58.6	1027	91.2

6. CONCLUSIONS

This paper has proposed a novel converter based on push–pull DC/DC converter for battery sourcing applications in transformer-less single phase inverter. This specific architecture provides high efficiency and high step-up DCDC conversion with the possibility of an independent adaptation single link to the converter ratio of the

transformer. In the paper, analysis of the converter has been presented in detail, from which design equations and circuit parameters were derived. The proposed converter can be operated with PWM control and constant switching frequency 20 kHz. Experimental results have verified that the proposed converter can achieve high efficiency over a wide load range. The proposed converter achieves a high efficiency of 91.2 % for its rated power. This paper proposed a new control schemes for push-pull DC/DC converter anDC/AC inverter, which allows to keep DC link and output voltage stable under input voltage and load variations, that ripple of Dc link is less than 1.5%. Moreover, the control scheme reduced transience time. The suggested converter is expected to be a good candidate for a standalone UPS, and PV application.

Thiết kế bộ nguồn cung cấp liên tục trên cơ sở bộ biến đổi DC/DC Push-Full hiệu suất cao

- **Lê Minh Phương**
- **Phan Quốc Dũng**
- **Nguyễn Minh Huy**
- **Nguyễn Hoài Phong**

University of Technology,VNU-HCM

TÓM TẮT:

Bài báo trình bày việc sử dụng bộ biến đổi DC/DC push-pull cho bộ nguồn cung cấp liên tục. Trong đó có đánh giá phân tích các cấu hình DC/DC truyền thống, chỉ ra những ưu điểm và nhược điểm. Đồng thời, lựa chọn bộ DC/DC push-pull với điều chế động cho cấu hình, trong đó ưu điểm chính là khả năng điều khiển và phân phối công suất từ nơi có điện áp thấp đến nơi có điện áp cao. Nhờ cấu hình đề xuất, mà tổn hao đóng ngắt giảm và vì vậy tăng hiệu suất của hệ thống. Bài báo cũng trình bày sơ đồ điều khiển cho bộ DC/DC push-pull và bộ nghịch lưu áp 1 pha DC/AC. Cấu hình bao gồm bộ DC/DC push pull hiệu suất cao và bộ nghịch lưu áp DC/AC được mô phỏng bằng cách sử dụng phần mềm Matlab/Simulink và được tiến hành thực nghiệm trên cơ sở DSP Piccolo TMS320F28027. Kết quả cho thấy khả năng đáp ứng tốt của điện áp DC link và điện áp tải AC khi tải thay đổi từ không tải đến tải định mức. Hiệu suất của mô hình 1kW 50Hz, 220-230VAC với nguồn cung cấp là 2 ắc quy mắc nối tiếp đạt được là: bộ DC/DC Push-

pull có hiệu suất 93,0%, và toàn bộ hệ thống đạt hiệu suất 91,2% trong đó độ méo dạng của điện áp tải AC đạt 1,9%.

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