

A LOW DROPOUT LINEAR VOLTAGE REGULATOR CHIP, THE TH7150

Ho Quang Tay and Ngo Duc Hoang

Ic Design Research & Education Center (ICDREC), VNU-HCM

ABSTRACT: A low dropout (LDO) linear voltage regulator, dubbed TH7150, is designed and reported. TH7150 is a power management device for analog chips, operating at low quiescent current ($100\mu A$), low voltage supply (1.6-3.6V), with low dropout voltage (200mV), and capable of driving 150mA output current. Its output voltage is programmable by logic control and also manually adjustable. It features protection measures for overheating and overloading and monitoring for the output voltage to prevent a dropout greater than 10% of current value. The chip is designed to be fabricated using $0.35\mu m$ process. It can be used as a standalone chip or integrated in a power supply chip for portable devices such as Smart phone, cell phone, Ipod, digital camera etc.

Keywords: LDO, low dropout linear voltage regulator, power management, overheating protection, low voltage supply, wide range voltage supply.

1. INTRODUCTION

Li-ion rechargeable battery is used in many electronic devices, but the output voltage is not stable. Typically, the full output voltage charge is 4.2V and when the battery is dropout, the voltage is just 2.7V. Due to this wide variation range, a regulator is needed to stabilize the supply voltage.

On the other hand, in a systems-on-chip (SoC), each IP (Intellectual Property) may need a different supply voltage. A power management is therefore needed here to manage the supply voltage for each IP.

A power management unit contains several IPs including regulators, logic controls and even an AD converter.

In this paper, we focus on the design of the regulator. There are two kinds of regulator: linear and switching regulators. The former is our main concern here. The main feature of a regulator is to provide a constant voltage supply.

The conventional 78xx series linear regulator is being widely used in many application boards. A disadvantage of this topology is the need of a high voltage dropout ($>1V$). This leads to high power dissipation. Switching topology helps reducing this heat. But the on/of switching frequency of the transistor becomes a source of noise for the SoC.

The LDO voltage regulator topology has been proposed and developed in recent years [1] as a solution to above problems. It does not generate the switching noise because it does not use an oscillator and with the low dropout voltage, the power dissipation is low and does not pose a heat problem.

In the following, the architecture and some circuits of the TH7150 are described and discussed in section II and the resulting layout for fabrication is introduced in section III, respectively.

2. ARCHITECTURE.

The functional diagram of the TH7150 chip is illustrated in Fig. 1. Its detailed specification is reported in [2].

The functional diagram of the TH7150:

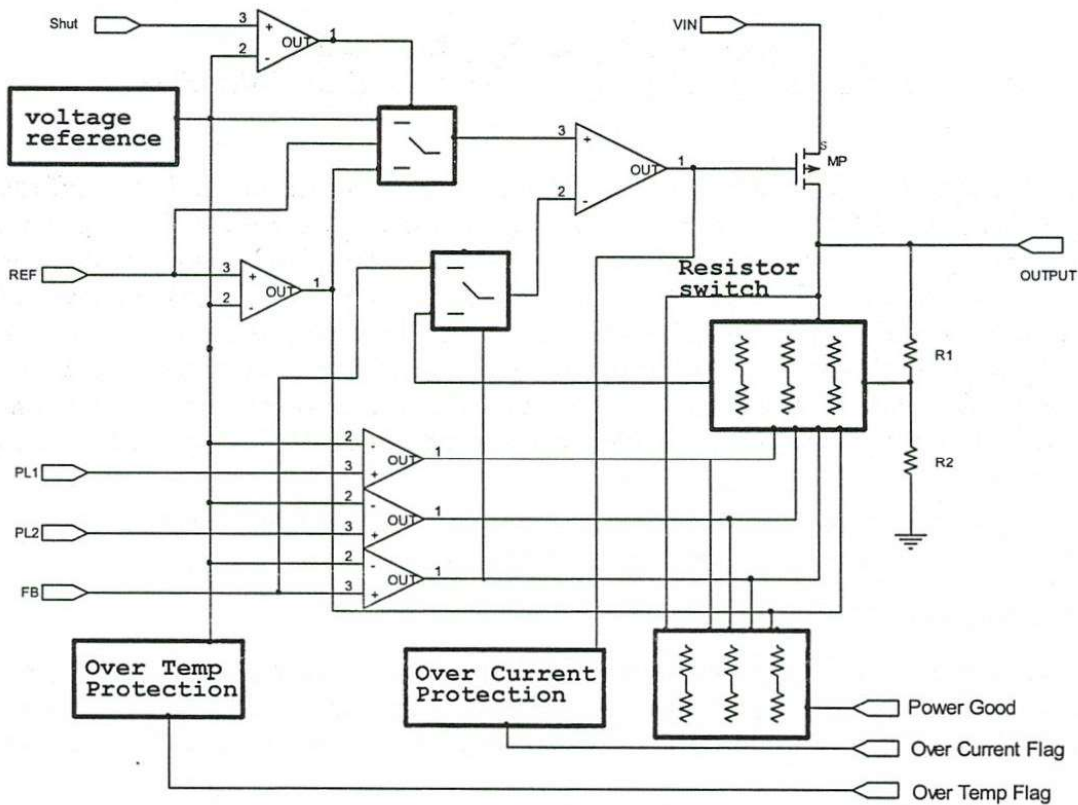


Fig 1. Functional diagram of TH7150

The port diagram of TH7150:

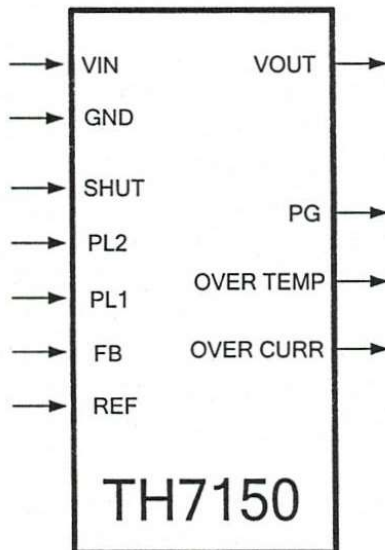


Fig 2. Port diagram of TH7150

The TH7150's output voltage is programmable or adjustable as shown in Table 1 where logic '0' and logic '1' correspond to a voltage smaller than 0.2V, and larger than 0.2V, respectively.

Table 1. The table operational of output voltage:

FB	REF	PL1	PL2	Vout
0	0	0	0	1,8 V
0	0	0	1	2,5 V
0	0	1	0	2,85 V
0	0	1	1	3,0 V
0	1	0	0	1,8 * Ref
0	1	0	1	2,5*Ref
0	1	1	0	2,85*Ref
0	1	1	1	3,0*Ref
1	0	X	X	$(1+R_1/R_2)*1.2V$
1	1	X	X	$(1 + R_1/R_2)*Ref$

3. TH7150 CIRCUIT DESIGN

Due to the page limit, we will only focus on some main blocks. For more detail, please refer to ref. [2].

3.1. Low Power Bias Circuit.

In an analog IC, the bias circuit is the most important block of the design; its main function is to generate the bias current (voltage) for all components in the design.

Many bias circuit topologies are available. But with the requirement for low voltage supply (1.6V) and wide voltage range (1.6V to 3.6V), the design becomes a difficulty, especially when it is also required to obtain a stable current.

In [3][4], a bias circuit was introduced that can generate a reference current that independent with temperature. We modify it to work in low voltage, the value of current through V_{DS} in each of transistor is:

$$I_B = \frac{V_{BE1}}{R} \quad (1)$$

The resulting circuit and simulation result for its output characteristics are shown in Fig. 3 (a) and (b), respectively.

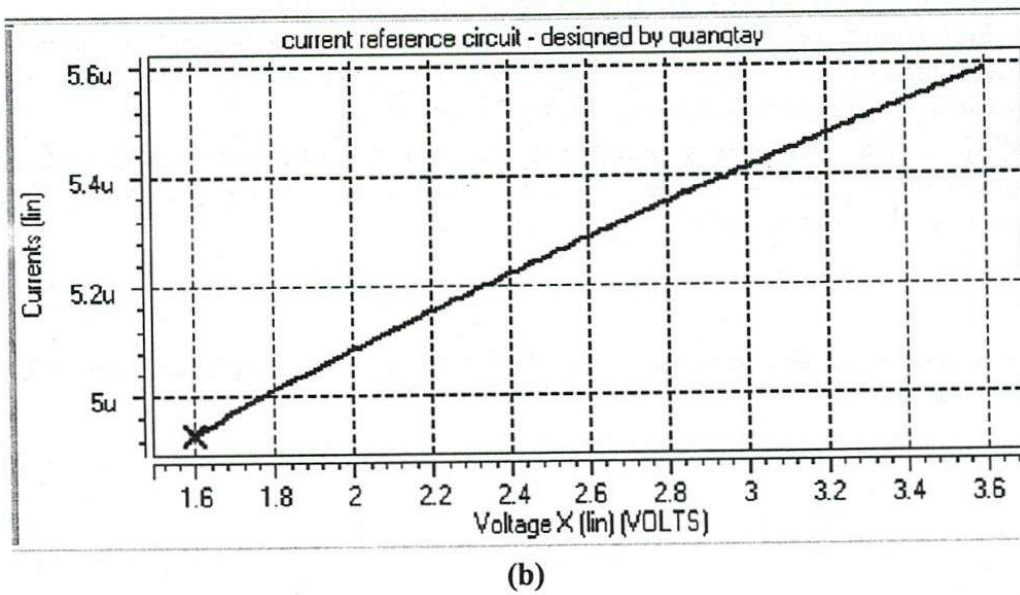
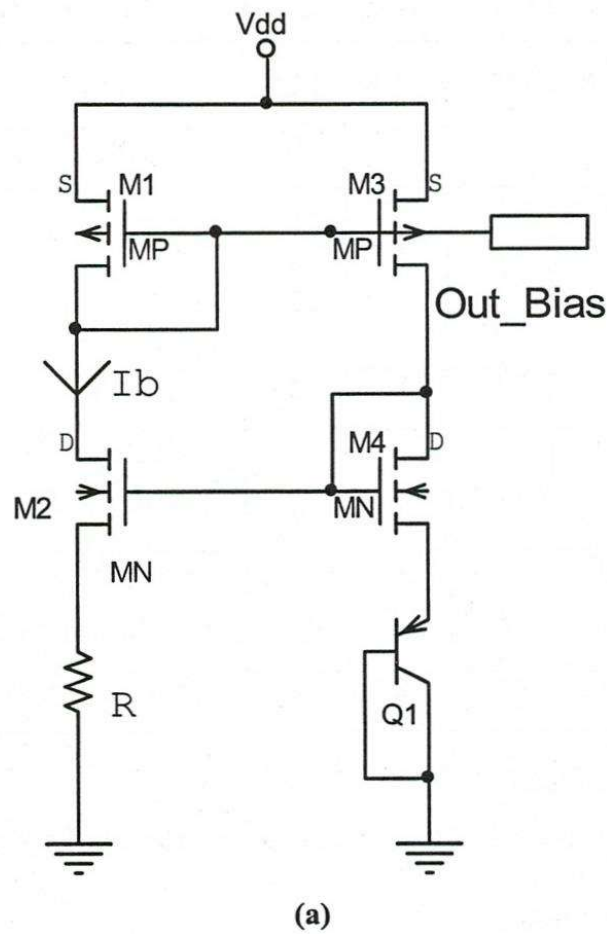


Fig 3. Current bias circuit (a) and simulation (b).

3.2. Stable Op Amp with Low Voltage Supply.

The op amp (operational amplifier) is a basic circuit of an analog IC. In order that an op amp can operate stably, its phase margin must be larger than 0. Among the many kinds of amplifier topologies, we choose the 2-stage one since it satisfies the above requirement. In the 2-stage op amp, the compensation capacitance and resistance for stabilization do not depend on the voltage supply [5], as shown below.

$$C = \frac{g_{m7}}{\omega_z} \quad (2)$$

$$R = \frac{1}{g_{m7}} (1 + (C_{db2} + C_{db4} + C_{gs7} + C_{db6} + C_{db7})/C) \quad (3)$$

The resulting circuit of the op amp is shown in Fig. 4.

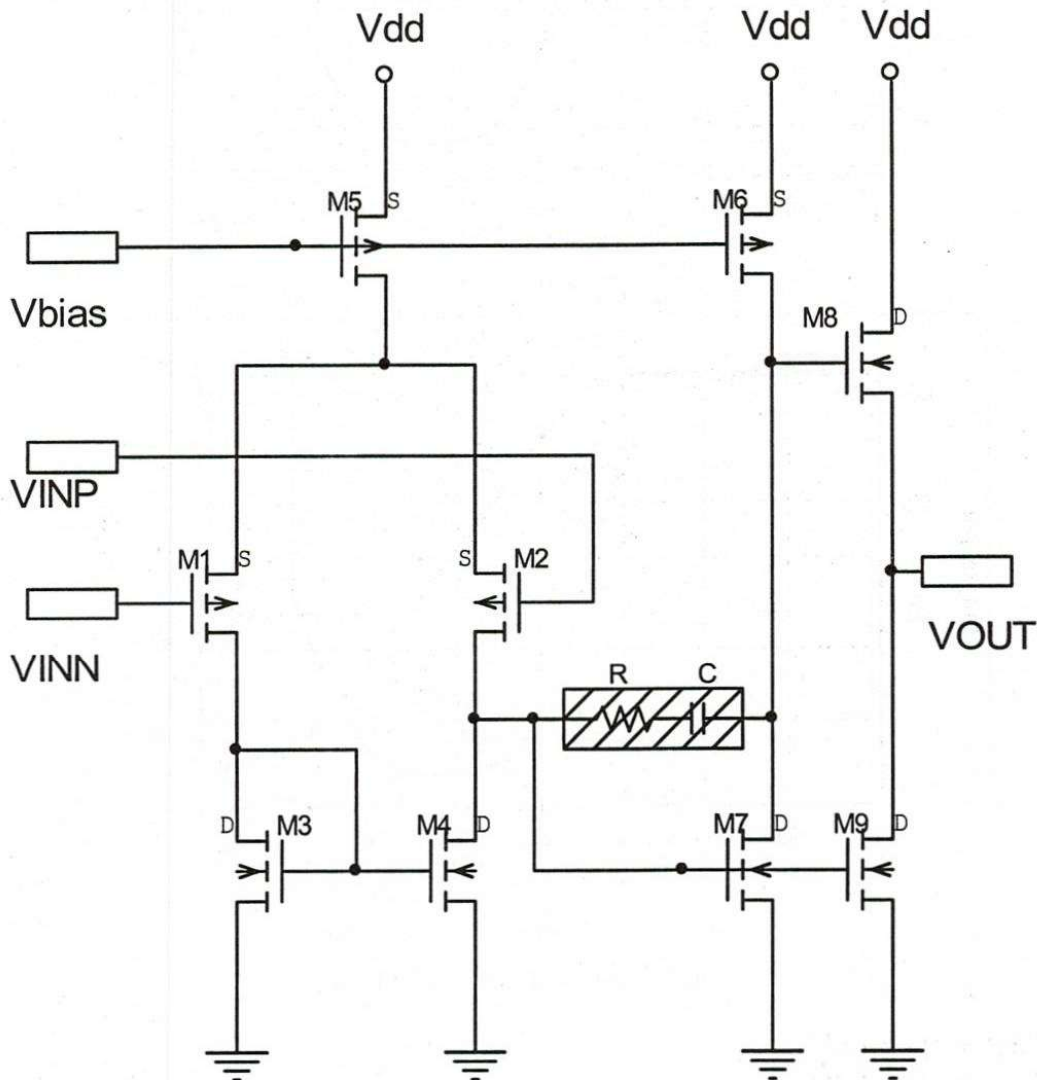
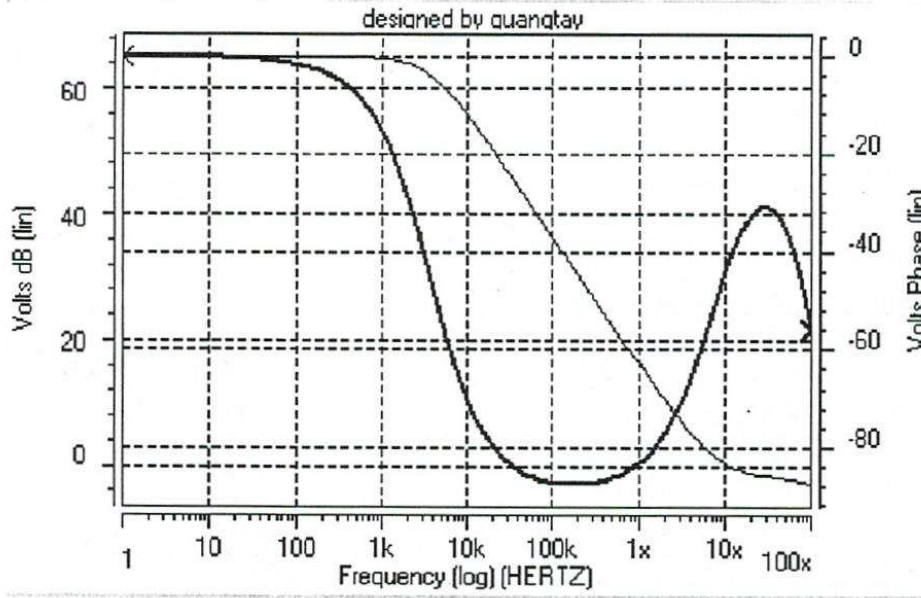


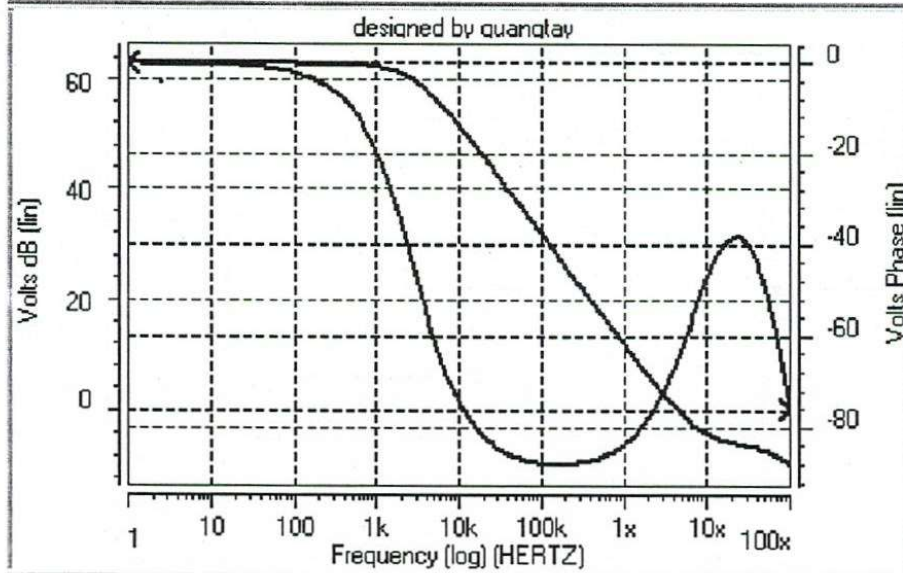
Fig 4. Two stage amplifier

The key improvement here is that the RC branch between the drain and the gate of M7 is designed as separate elements to reduce the influence of the supply voltage.

Two simulation results corresponding to 1.6V and 3.6V voltage supply, respectively, are performed and shown in Fig. 5. As can be seen, the requirement for a phase margin larger than 0 is clearly obtained.



(a)



(b)

Fig 5. Result amplifier simulation.

Voltage supply: 1.6V.

Voltage supply: 3.6V.

3.3. Bandgap Voltage Reference.

The bandgap voltage reference circuit is based on Ref.[6]. It is shown below in Fig. 6 for completeness.

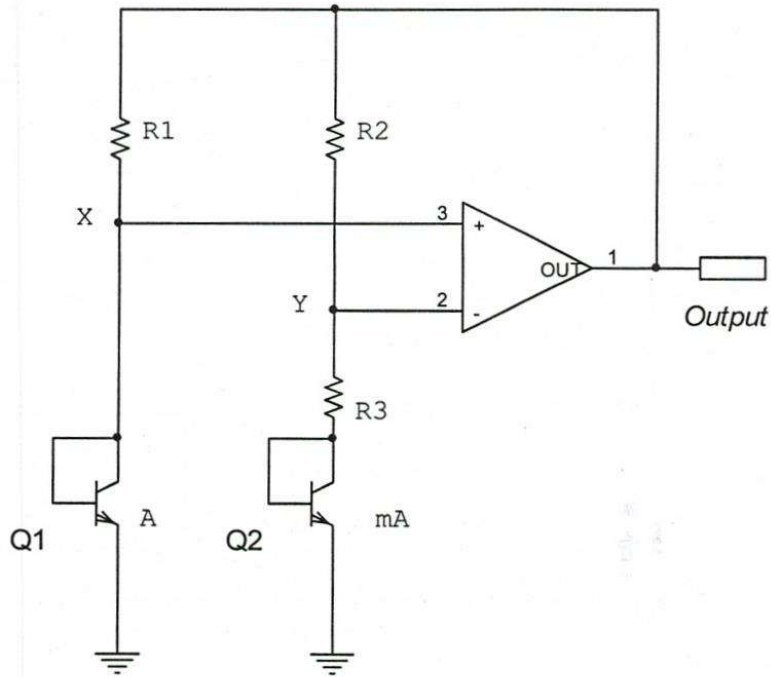


Fig 6. Bandgap reference voltage circuit.

The output voltage is given as follows.

$$V_{output} = V_{EB} + \left(1 + \frac{R_2}{R_3}\right) \frac{KT}{q} \ln m \quad (4)$$

In our design, V_{output} value is found to be 1.222V.

In the simulation shown in Fig. 7, the bandgap voltage changes very little throughout a wide range of temperature so that it can be considered as constant.

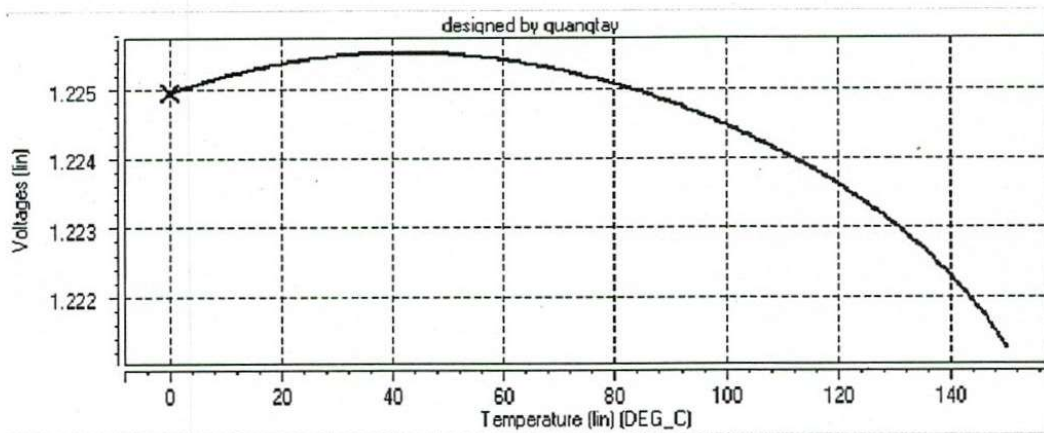
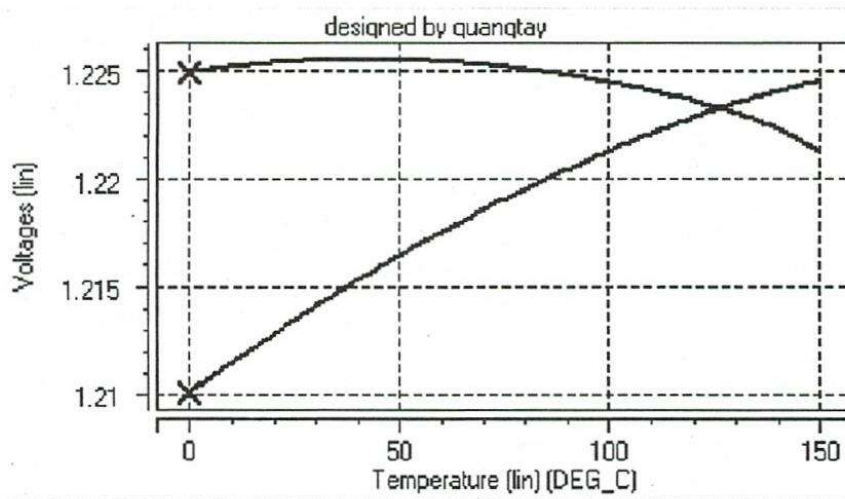
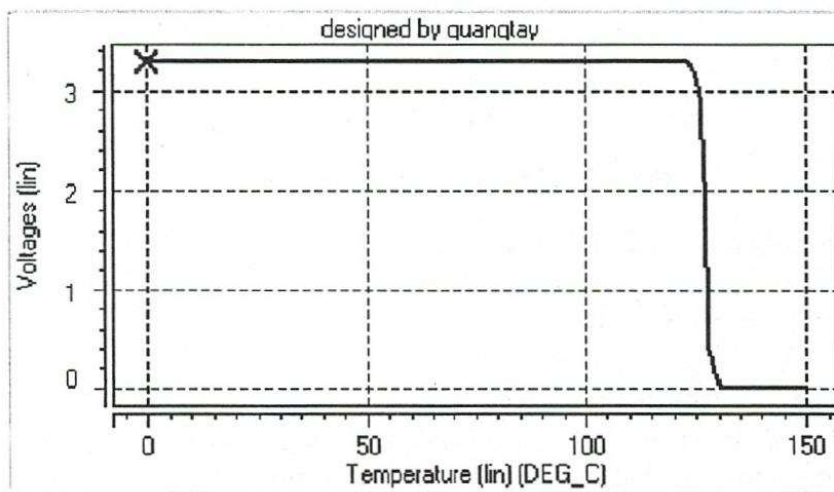


Fig. 7. Bandgap voltage reference with temperature.

The simulation in Fig. 7 is only shown the output of bandgap is stable with temperature. That value is also stable with voltage supply. With those feature, the over temperature protection application is created as the simulation result in Fig. 8.



(a)



(b)

Fig 8. The result of over temperature protection.

Operational over temp protection.

Over temp protection flag.

3.4. Low Dropout Voltage Architecture.

Basically, Low dropout voltage regulator is a negative feedback amplifier with an input is the bandgap voltage reference. Let consider the topology of regulator in Fig. 9

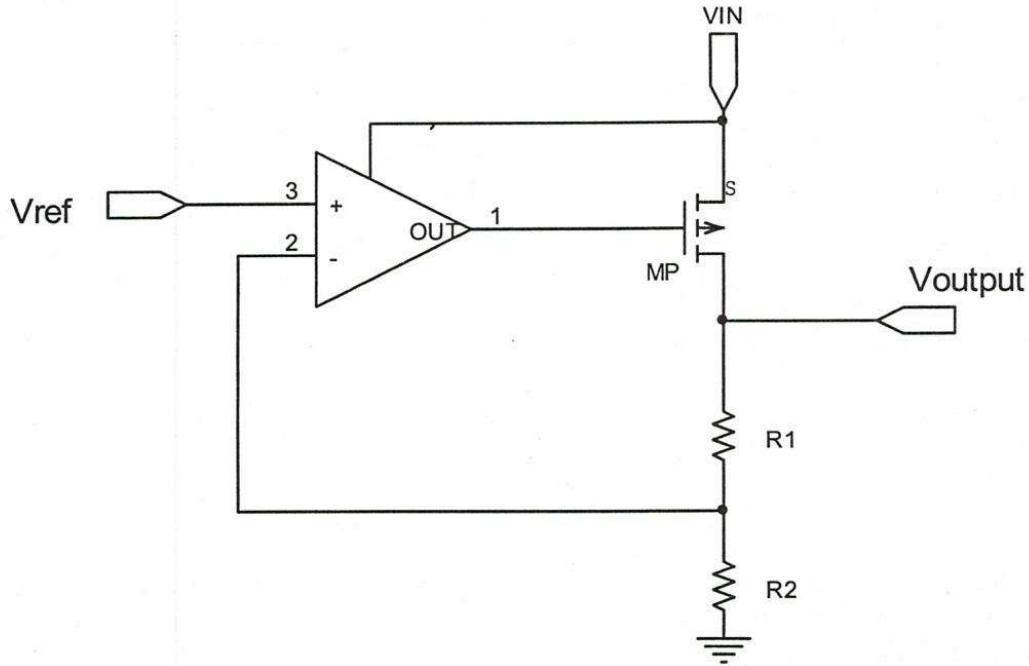


Fig 9. Topology of LDO regulator.

This is basically a DC feedback amplifier. From [1] [7], we have:

$$V_{output} = V_{ref} \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

If we fix the value of V_{ref} , R_1 and R_2 , the output voltage will be unchanged. The value of bandgap reference is calculated in (4), the value of R_1 and R_2 will be calculated through the output voltage and ground current.

The parameters of the MP transistor can be found to be given by Equation (7) as follows.

$$I_D = \frac{\mu_p C_{ox} W}{2 L} (V_{sg} + V_{tp})^2 \quad (6)$$

Therefore

$$I_D = \frac{\mu_p C_{ox} W}{2 L} V_{dropout}^2 \quad (7).$$

With our specification and using, for example, TSMC 0.35 μ m process technology, the pass device is defined with $L = 0.4\mu$ m and $W = 19\mu$ m.

The result in Fig. 10 shows that the output voltage is 3V when the voltage supply is greater than 3V.

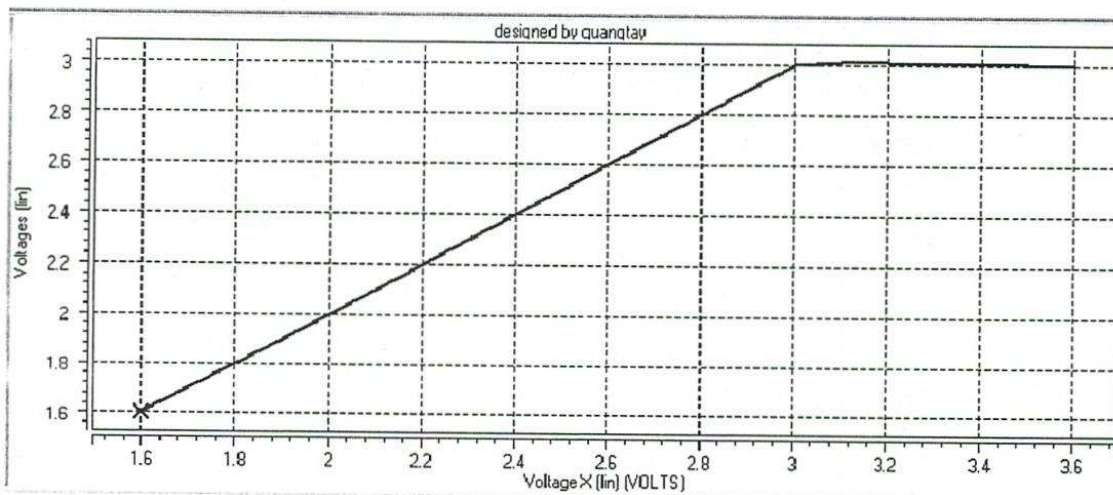


Fig 10. Output voltage of LDO.

It can be seen that all output voltage levels in Table 1 will be defined depending on the R_1 and R_2 . Therefore, the voltage of output can be chosen by using an analog switch and a resistance network feedback.

4. PHYSICAL DESIGN (LAYOUT).

The physical design is accomplished routinely in CosmosLE environment offered by Synopsys.

The transistor pass is the most importance device of the TH7150 chip. This transistor, as designed is rather big ($W=19\mu\text{m}$ and $L=0.4\mu\text{m}$).

When the layout of TH7150 is done, we must verify to check the DRC and LVS error by using Hercules. After that, we use the Star-RCXT to extract the parasitic (Resistance and capacitance), back annotation simulation to check functions of the design in layout level.

When these functions meet the specification, we tape out the project through the MOSIS educational program. The total area of this chip include IO Pad is $2.7\text{mm} \times 2.7\text{mm}$. The micrograph of TH7150 is shown in Fig. 11.

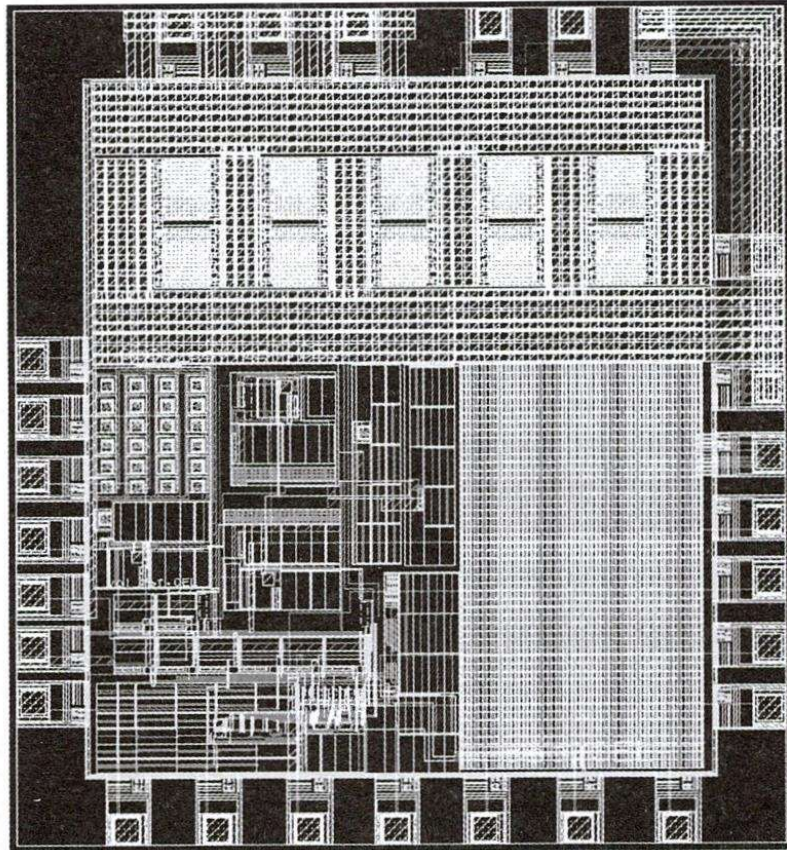


Fig 11. Layout of TH7150

5. CONCLUSION

We have succeeded in designing a low dropout linear voltage regulator chip which we named TH7150. As simulated, the new chip proves to meet all design targets, namely low operating current and voltage, low dropout voltage, high output current, ease of output voltage controlling, either logically or manually, and featuring protection measures for overheating and overloading.

Due to page limitation, we can not introduce all parts and components of the design, but we have concentrated on most important ones that help giving rise to the desirable characteristics as shown.

The trial fabrication of prototype chips was entrusted to a well-known foundry (the TSMC – Taiwan Semiconductor Manufacture Company Ltd.). The first test chips were checked to meet all design targets. Detail of this measurement will be report in a future paper soon.

We are furthering our improvement to upgrade functional blocks of the TH7150 to increase the output current from 150mA to 500mA and to design a new ESD (Electronic Static Discharge) circuit to protect the chip. This will make the subject of our next report.

6. ACKNOWLEDGEMENT

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VI MẠCH ỔN ÁP TUYẾN TÍNH ĐIỆN ÁP RƠI THẤP, TH7150.

Hồ Quang Tây, Ngô Đức Hoàng

Trung tâm Nghiên cứu và Đào tạo Thiết kế Vi mạch (ICDREC), ĐHQG-HCM.

TÓM TẮT: Vi mạch ổn áp dạng điện áp rơi thấp (LDO) với tên TH7150 đã được thiết kế. TH7150 là thiết kế vi mạch tương tự mà có thể được xem như một bộ quản lý nguồn đơn giản. Nó hoạt động với dòng đất thấp ($100\mu A$), điện áp thấp (1.6-3.6V), điện áp rơi thấp (200mV), và có thể lái dòng tải 150mA. Điện áp ngõ ra có thể lập trình bằng các chân điều khiển hoặc điều chỉnh được. TH7150 còn có đặc tính bảo vệ như: bảo vệ quá nhiệt, quá tải và giám sát hoạt động (không cho phép giá trị điện áp ngõ ra rơi quá 10%). TH7150 được thiết kế và chế tạo dựa trên công nghệ $0.35\mu m$. Nó có thể hoạt động dạng độc lập hoặc tích hợp vào trong chip cho các ứng dụng như: điện thoại di động, PDA, Ipod ...

Từ khóa: LDO, vi mạch ổn áp, điện áp rơi thấp, quản lý nguồn, bảo vệ quá nhiệt, nguồn điện áp thấp

REFERENCES

- [1]. Chava C.K., Silva-Martinez, J., A Frequency Compensation Scheme for LDO Voltage Regulators, IEEE Transactions, vol. 51, no. 6, pp. 1041 – 1050, Jun. 2004.
- [2]. ICDREC, Research, design and manufacture a prototype of RISC 8 bit HN-07 microprocessor and TH7150 LDO regulator IP, scientific report, 2009 [Online] Available: <http://www.icdrec.edu.vn>.
- [3]. Li Yanming, Lai Xinquan, Jia Xinzhang, Novel Temperature Stable CMOS Current Reference, Proceeding of 8th ICSICT, pp. 1772 – 1775, 23-26 Oct. 2006.
- [4]. G.A Rincon Mora and P.E Allen – A low voltage, low quiescent current, low drop-out regulator – IEEE J. Solid State Circuits, vol. 33, no. 1, pp. 36 – 44, Jan.1998.
- [5]. David Johns, Ken Martin, Analog Integrated Circuit Design, ed. John Wiley & Sons, New York, pp. 221 – 250, 1996.
- [6]. Behzad Razavi, Design of analog CMOS Integrated circuits, ed. Mc Graw-Hill, pp. 381 – 389, 2000.
- [7]. Milliken R.J., Silva Martinez J., Sanchez-Sinencio, Full On-Chip CMOS Low-Dropout Voltage Regulator, IEEE Transactions, vol. 54, no. 9, pp. 1879 – 1890, Sept. 2007.