HN-07 MICROPROCESSOR – THE SECOND VIETNAMESE MICROPROCESSOR

Ngo Duc Hoang, Hau Nguyen Thanh Hoang, Ngo Quang Vinh, Duong Van Khanh, Nguyen Phu Quoc, Pham Thanh Hung, Do Hoang Sang, Nguyen Van Binh
IC Design Research & Education Center, VNU-HCM

ABSTRACT: *After the first success with SigmaK3 [1], we have designed and developed the second 8-bit microprocessor chip, dubbed HN-07, with high performance and additional features. HN-07is based on the original Sigmak3 architecture with a number of improved features, namely 5-stage pipeline architecture, interrupt controller, more on-chip peripherals, higher operational stability and frequency. This improved architecture makes HN-07 microprocessor equivalent with others such as Intel 8051, Microchip PIC, etc. Our complete design, from front-end through back-end stages, has been taped out and supplied to an overseas foreign foundry for trial fabrication. Further detail on the evaluation of its performance will be reported in the future.*

Keywords: *microprocessor, RISC, computer architecture, pipeline*

1. INTRODUCTION

A microprocessor is a small computer on a single integrated circuit consisting of a CPU and a number of functional blocks, namely a crystal oscillator, timers, a watch-dog, serial and analog I/O circuits, etc. Microprocessors are used widely in almost all electronic equipments. Some of most popular microprocessors are PIC (Microchip), AVR (Atmel), ARM (ARM), Alpha (DEC), PA- RISC (HP), SPARC (Sun Microsystems), MIPS (MIPS Technologies), and PowerPC (IBM), etc.

According to a recent report [2], the consumption of semiconductors in Vietnam will amount to US$ 1.8 billion by 2011. This may serve as a basis for possible future investments, domestic and foreign, to turn Vietnam into a next manufacturing power and a sizable economic force in a near future. To date in Vietnam, domestic companies develop their own applications utilizing microprocessors designed and fabricated by foreign vendors. There does not exist a made-in-Vietnam microprocessor.

In that situation, ICDREC pioneered to lay the foundation for designing and developing IC's and succeeded in designing and manufacturing the first 8-bit RISC microprocessor SigmaK3 (KC01 project, the Technology Cultivate Seedlings program). The feat was counted as one of ten 2008 outstanding science-technology events in Vietnam [3]. Our further research to improve its performance has led to the new microprocessor HN-07 featuring salient improvements, and operating at higher frequency and stability.

Our purpose in this paper is to present thoroughly the new architecture of microprocessor HN-07 in comparison with other microprocessors in the world market in section 2. Then we describe in detail the design flow to develop our microprocessor HN-07, in section 3. Finally, we draw some conclusions and perspectives in section 4.

2. THE ARCHITECTURE OF MICROPROCESSOR HN-07

2.1 Overview

As its predecessor, SigmaK3, the microprocessor HN-07 is targeted as a low-cost, high performance low power consumption 8-bit CPU employing a modified RISC architecture with separate instruction and data buses. This allows a simultaneous access to program and data memories. The 5-stage pipeline allows HN-07 to perform 5 instructions at the same time, resulting in a net processing speed 5 times faster than a normal pipeline-less architecture. All instructions are executed in one system clock cycle, except branch instructions in 2 cycles.

Furthermore, a dedicated compiler is developed specially for HN-07 in order to exploit HN-07 pipeline architecture to optimize instruction arrangement. This also improves the microprocessor's performance.

CPU's features

- Harvard RISC 5-stage pipeline architecture
- 37 instructions.
- 14-bit instruction width.
- Extensible instruction memory up to
- 64Kx14-bit
- Power saving SLEEP mode. Synchronous design.

Peripherals

Interrupt controller: 8 interrupted sources

- External interrupts.
- Changing input values port interrupts.
- Timer0 interrupt.
- Timer1 interrupt.
- Timer2 interrupt.
- USART received interrupt.
- USART transmitted interrupt.
- CCP interrupts.

Four 8-bit bidirectional I/O ports.

Timer0: operate at two modes: Timing mode (using system clock signal) and counter mode (using external clock signal). 8-bit Timer0 can be increased to 16 bits by combining with 8 bit programmable prescaler register.

Timer1: operate at two modes: Timing mode (using system clock signal) and counter mode (using external clock signal). 16-bit Timer1 can be increased to 19 bits by combining with 3 bit prescaler register.

Timer2: operates only at timing mode (using system clock signals). 8-bit Timer2 can be increased to 16 bits by combining the postscaler and the prescaler registers. CCP1 (Compare Capture PWM – Pulse- Width Modulation)

- 16 bit Comparator.
- 16 bit Capture.
- 10 bit resolution PWM.

USART (Universal Synchronous

Asynchronous Receiver Transmitter), operate at 3 modes:

- Asynchronous Mode – full duplex transmission.
- Synchronous Master Mode – haft duplex transmission.
- Synchronous Slave mode – half duplex transmission.

Watchdog Timer (8-bit)

- Configurable time-out range.
- Can be increased to 15 bits bycombining with 7 bit prescaler register.
- Use a particular clock signal independent with system clock signal.

Table 1 shows the detailed comparison between the microprocessor HN-07 and two others, the AT89C52 (ATMEL) and the PIC16C67 (MicroChip). We can see that HN-07's maximum frequency is 100MHz, much higher that of the two others. The parasitic capacity effect on HN-07 was calculated to prove its proper operation at 100MHz. Moreover, HN-07 has a data memory size 2.0 and 1.4 times larger than that of AT89C52 and PIC16C67, respectively. Similarly, HN-07 has a instruction memory size 7 and 4 times larger than that of AT89C52 and PIC16C67.

Table 1. Comparison between microprocessor HN-07 and two microprocessors AT89C51 and PIC16C67

Microprocessor	AT89C52 (ATMEL)	PIC16C67 (MicroChip)	HN-07 (ICDREC)
Architecture	CISC	RISC	RISC
Instruction memory	8K x 8 bit	8K x 14 bit	32K x 14 bit
Data memory	256 x 8 bit	368 x 8 bit	512 x 8 bit
Frequency	24 MHz	20 MHz	100 MHz
Pipeline	No	2 stages	5 stages
clock cycles / instruction	12	4	1
Peripheral	I/O PORTs TIMER UART INTERRUPT	I/O PORTs TIMERs WATCHDOG USART CCP SSP PSP INTERRUPT	I/O PORTs TIMERs WATCHDOG USART CCP INTERRUPT

2.2 HN-07's ports diagram

The HN-07 has 100 pins. The principal pins are shown in Figure 1. Table 2 describes in detail the name and the function of all ports. The HN-07 is divided into four main blocks: CPU block, RAM block, peripheral blocks and interrupt controller block, as shown in the Figure 2.

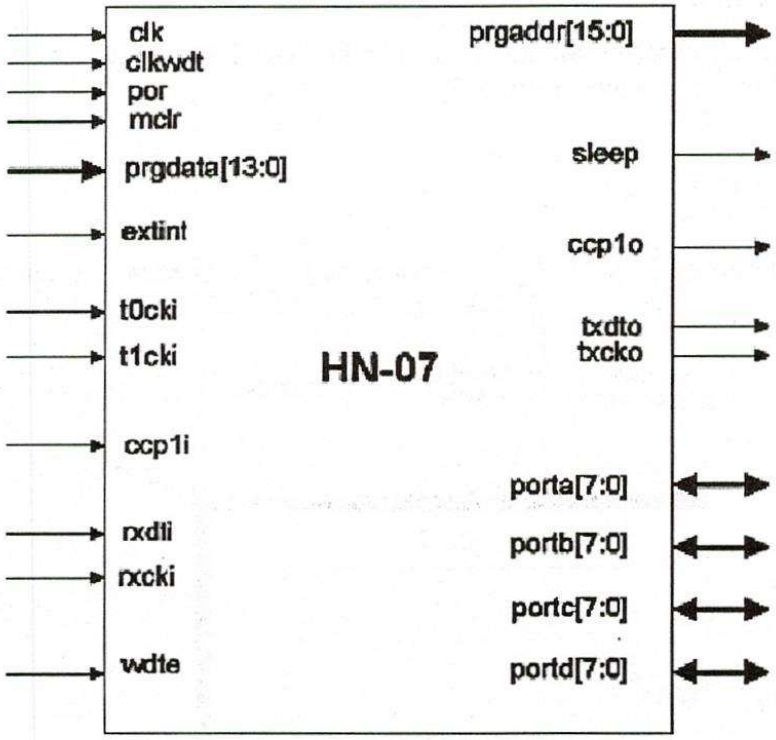

Figure 1. HN-07's ports diagram

Table 2. HN-07 port description

Port name	Direction	Description
clk	input	System clock
por	input	Power on reset
mclr	input	Master clear reset
clkwdt	input	Clock for Watchdog timer
prgdata	input	Program memory data bus
extint	input	External interrupt signal
t0cki	input	Timer0 clock in
t1cki	input	Timer1 clock in
ccp1i	input	CCP1's input
rxdti	input	USART Receive data in
rxcki	input	USART external clock in
wdte	input	Watchdog enable
porta	inout	Port a
portb	inout	Port b
portc	inout	Port c
portd	inout	Port d
prgaddr	output	Program memory address bus
sleep	output	Sleep/normal mode sleep
ccp1o	output	CCP1's output
txdto	output	USART Transmit data output
txcko	output	USART Transmit clock output

2.3 Block Diagram

The CPU block controls all the other blocks. The interrupt controller is an additional block compared to the previous SigmaK3.

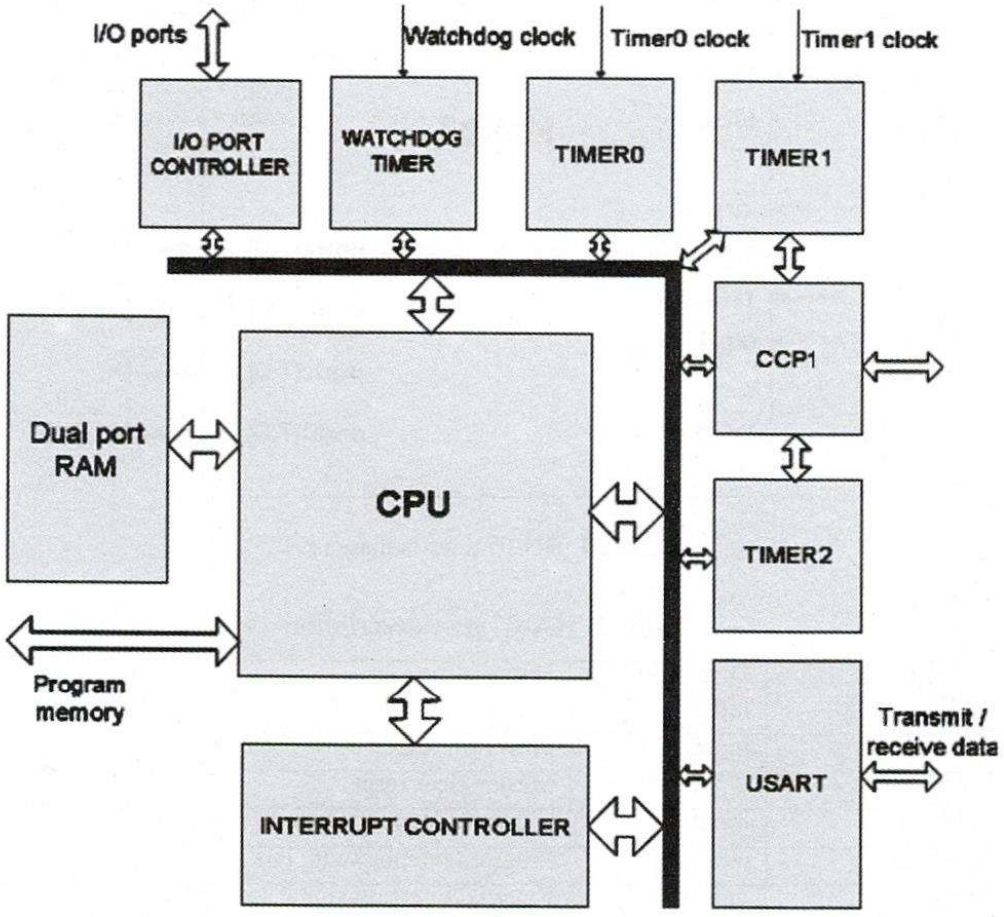

Figure 2. HN-07's block diagram

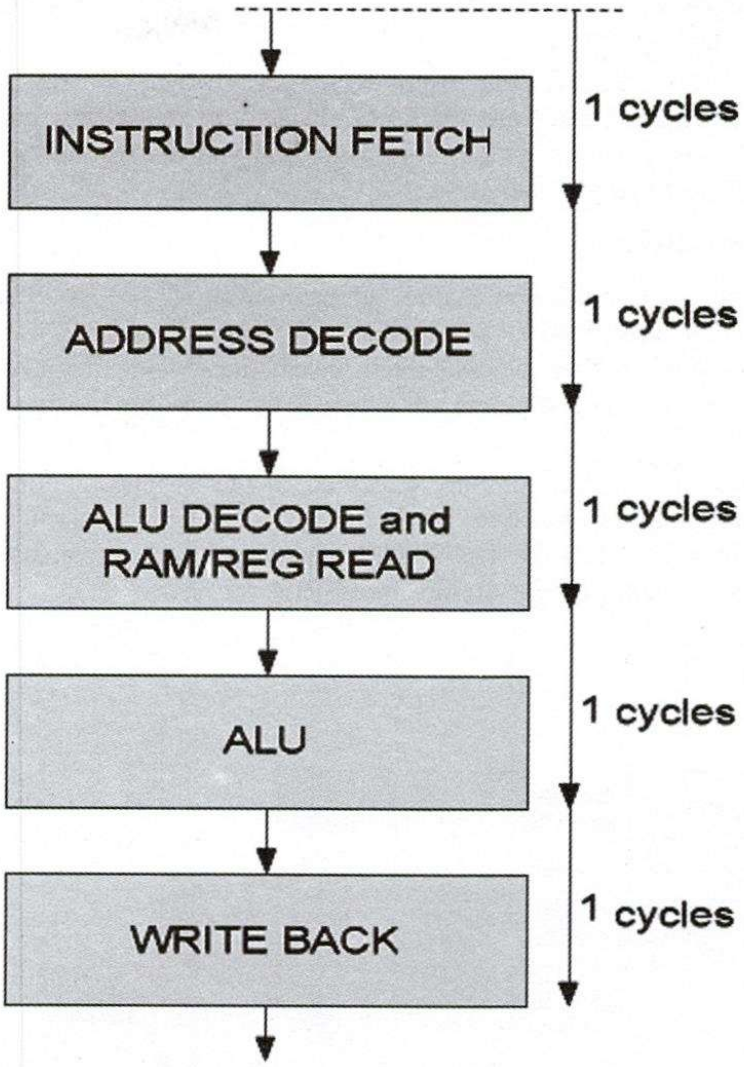

Figure 3. CPU's data path

2.4 CPU's data path

This section describes the execution process of a single instruction by the CPU. It takes 5 cycles to accomplish a single instruction, as shown in the Figure 3.

1. Cycle 1 INSTRUCTION FETCH: Instruction code is fetched from ROM to instruction register.

2. Cycle 2 - ADDRESS DECODE: RAM/ REG address is decoded by combining two parts: the 3 higher bits [7:5] of STATUS register and the address-field bits stored inside instruction code.

3. Cycle 3 - ALU DECODE and RAM/REG READ: includes two simultaneous operations: (1) ALU DECODE operation: decoding instruction and generating ALU controlling signals, write-enable signals, and other control signals. (2) RAM/REG READ operation: reading data from RAM or registers corresponding to the access address obtained in cycle 2.

4. Cycle 4 - ALU: performing arithmetic and logical operations. ALU accepts three inputs: (1) data from W register (Work register), (2) data from RAM/REG READ (in cycle 3) and (3) ALU controlling signals (in cycle 3).

5. Cycle 5 - WRITE BACK (the result from ALU in cycle 4 will be written into the destination): The destination can be RAM/REG, flags, sleep mode flag, etc. More detail, this writing operation need two information: (1) destination address resulted in the cycle 2, (2) write-enable signals resulted in cycle 3.

2.5. Pipeline architecture

The pipeline architecture is a new feature of our microprocessor HN-07 as compared to its predecessor, SigmaK3. With its 5-stage pipeline architecture the HN-07 can perform a multi-instruction executing. In other words, fetch instructions and memory transfer can be overlapped by the multi-stage pipeline to increase the microprocessor's effectiveness and performance.

Figure 4 shows how instructions are executed in the 5-stage pipeline architecture. We see that each instruction is executed in 5 clock cycles and 5 instructions are executed simultaneously. This means that the HN-07 CPU has a performance increase of five times in comparison with other non-pipeline architecture CPUs.

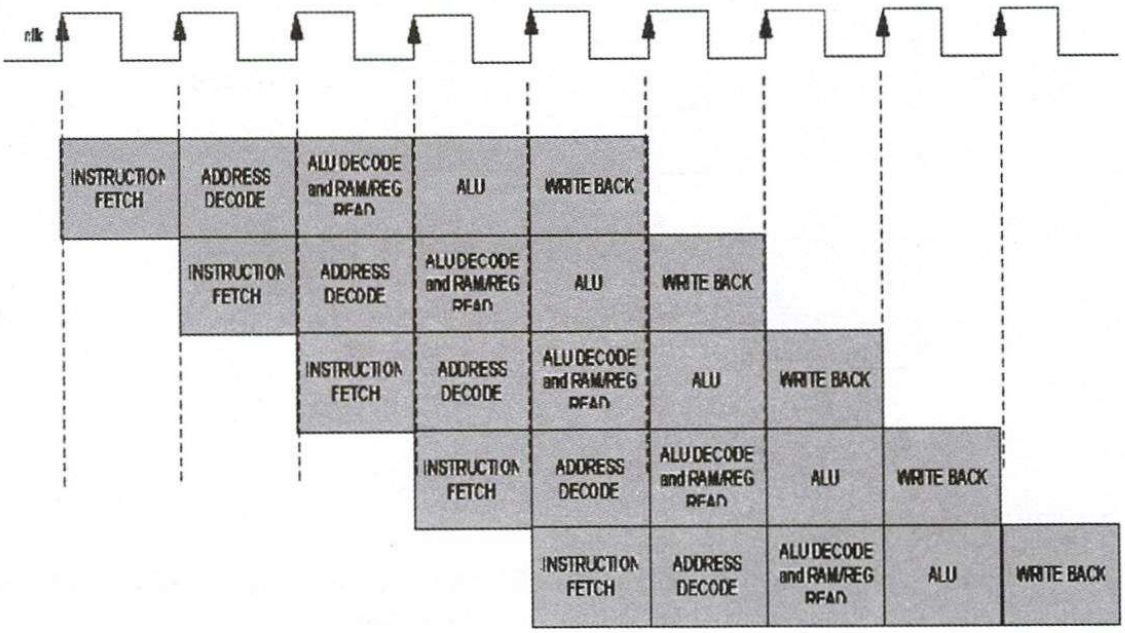

Figure 4. 5-stage pipeline architecture

2.6 Applications with microprocessor HN-07

Similar to traditional 8-bit microprocessors, the microprocessor HN-07 can be used as a Central Processing Unit (CPU) for electronic equipments such as:

- Message Display System.
- Robot controller.
- Communication devices.
- Washing machine controller, TV remote controller.

- Product counting device.
- Telephone switchboard, electronic watch, LCD display
- ID Analyzed and Recognized device. Many other electronic devices...

At ICDREC, we have developed our own applications using the microprocessor HN-07, such as: Message Display System, Robot controller, Washing machine controller, TV remote controller.

3. DESIGN FLOW

Microprocessor HN-07's design process follows standard digital design process using Synopsys software tools. The HN-07 is completely designed by ICDREC in Vietnam.

The design process includes two stages: Front-End and Back-End. The Front-End stage is usually called "Early Physical Design", or shortly "Design". The final product of this stage is the gate level netlist (after synthesis). The Back-End stage is called "Physical Design", or "Layout". The final product of this stage is a GDSII file. It is also the final product of the whole design process.

The GDSII file will be sent to manufacture at foreign foundries, such as MOSIS, UMC, IBM etc. Since there does not exist any chip fabricate company in Vietnam. In fact, we have sent our design HN-07 to manufacture at MOSIS in Singapore.

Font-End stage: include 5 steps

Step 1: System Specification Based on system requirements, this step analyzes and design system specification. System specification includes data flow, timing, ports diagram, functional description for each block, connecting all blocks together

Step 2: Function design This step is RTL coding (functional programming for each block) by using hardware description language such as Verilog, VHDL etc. For the HN-07, we use Verilog language.

Step 3: Logic design. Use Leda tool to check syntaxes or rules of the RTL codes. The purpose of this step is to facilitate the synthesis process at the next stage. We also use VCS tool to check the functional behavior of each block. If errors are detected, it must return to step 2.

Step 4: Logic verification. Combine all functional block together, use VCS tool to simulate, and check the functional behavior of entire chip at RTL level.

Step 5: Circuit Design. The Design Compiler (DC) tool is used to synthesize RTL-level design. We use VCS tool to check the functional behavior of entire chip at netlist level. If errors are detected, it must return to step 2.

The final product of Front-End stage is the gate level netlist of entire chip. This netlist file will be used to produce layout.

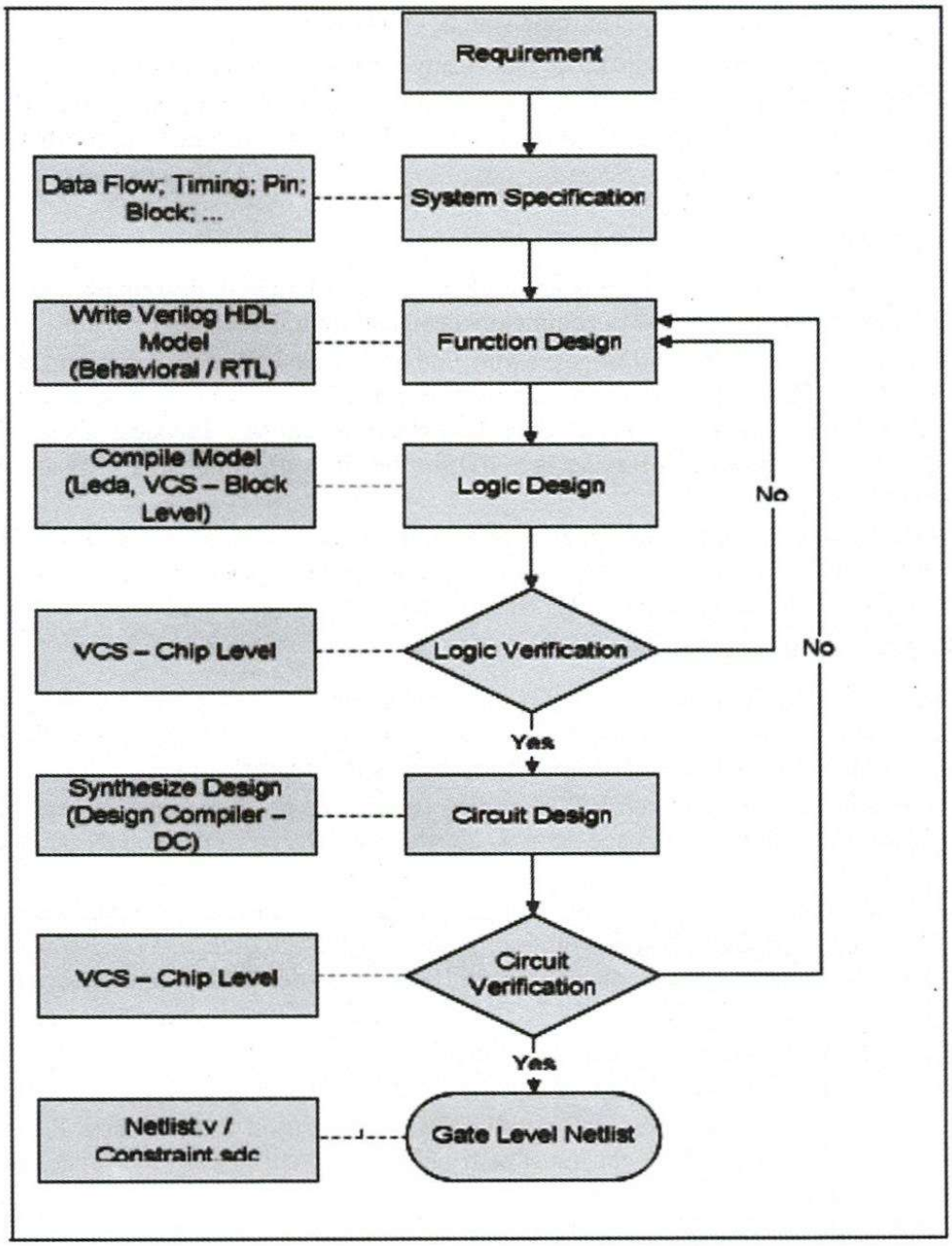

Figure 5. Front-End design flow

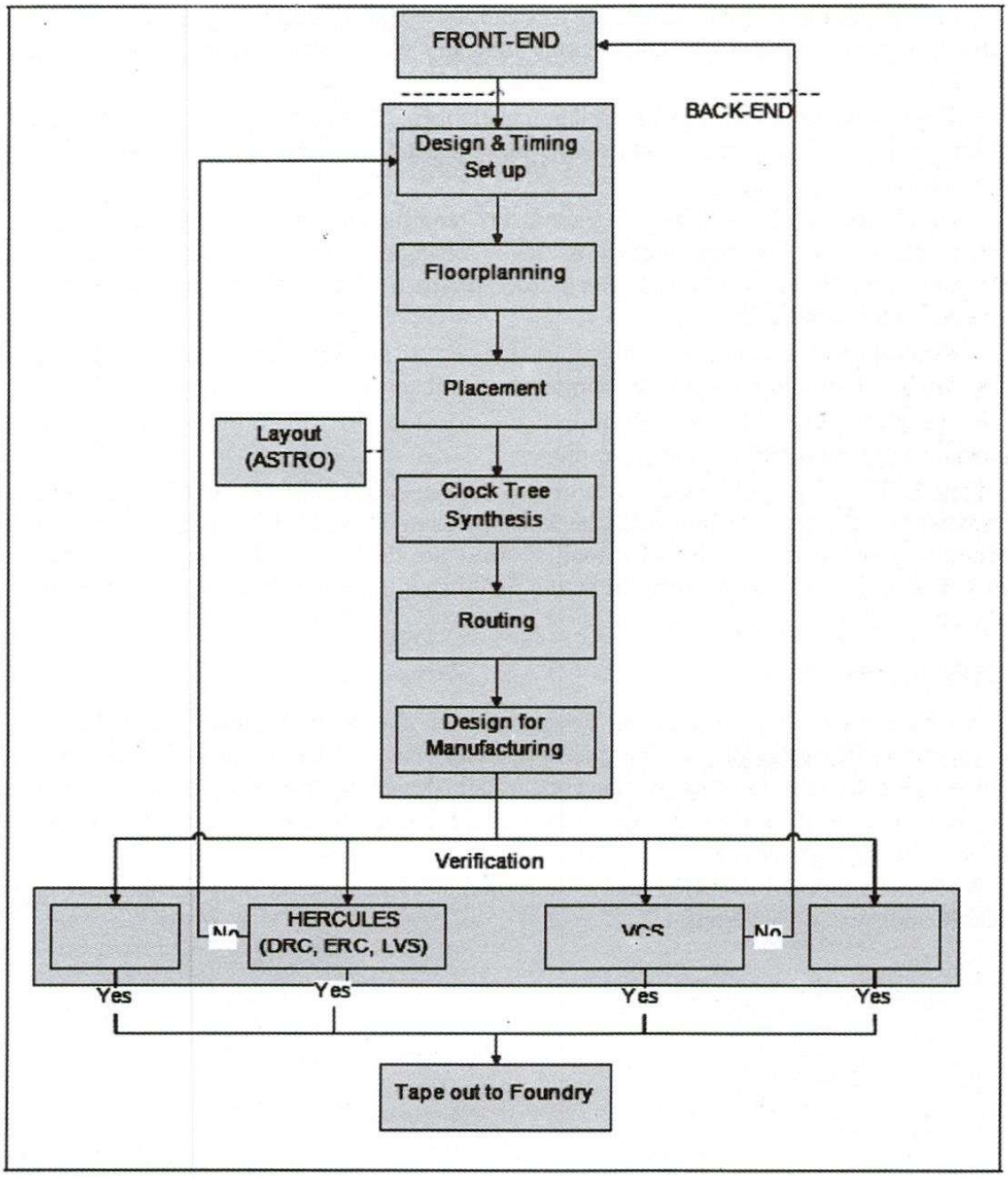

Figure 6. Back_End design flow

Back-End stage: include 2 steps:

Step 1: The layout producing process will be performed by utilizing the Astro tool. Inputs of Back-End stage are gate level netlist and constraints resulted from Front-End stage. The layout process is performed successively through 6 below sub-steps:

1. Design & Timing Set up: Create design libraries and start cells from the standard libraries of specific manufacturer in combination with netlist file and timing constraints from Front-End stage.

2. Floorplanning: Determine core area, create source pads, locate I/O pads and macro cells. Optimize macro-cells arrangement, arrange logically power grid and put blocks at suitable places.

3. Placement: Put cells into Floorplanning platform so that they don't violate congestion and timing issues. Carry out the cells auto-place process. Optimize one more time after auto-place process.

4. Clock tree synthesis: Establish parameters requirements for clock synthesis, determine implicit clock tree, terminal points to make changes when necessary. Control timing constraints in order to synthesize clock tree. Analyze clock's timing and other technical parameters after synthesis.

5. Routing: Auto-connect cells together. This process follows chip manufacture technical rules. Analyze both timing and other optimization adjustments.

6. Design for Manufacturing: Perform necessary steps after the previous process Routing: Antenna fixing, metal filling, metal slotting etc.

Step 2: The layout file, resulted from step 1, is checked LVS (Layout Versus Schematic comparison) and DRC (Design Rule Checking) by using Hercules tool. This layout file is also verified at post-layout level by VCS tool. If errors are detected in this step, it must return to step 1. Otherwise, this layout file will be the final result to send to foundry to manufacture the real chip.

4. CONCLUSION

We have briefly reported the IC design state-of- the-art in Vietnam through a detailed description of the design of the 8-bit microprocessor HN-07, a successor to the first design-in-Vietnam chip SigmaK3, from its concept through design flow and actual design work. As designed using well- known design tools, HN-07 proves to out-perform other established famous 8-bit microprocessors.

We believe that the ICDREC and its first products will pave the way for the development of the IC industry in Viet Nam.

VI XỬ LÝ HN-07 -- VI XỬ LÝ THỨ 2 CỦA NGƯỜI VIỆT NAM

Ngo Duc Hoang, Hau Nguyen Thanh Hoang, Ngo Quang Vinh, Duong Van Khanh, Nguyen Phu Quoc, Pham Thanh Hung, Do Hoang Sang, Nguyen Van Binh
Trung tâm Nghiên cứu và Đào tạo thiết kế vi mạch (ICDREC), ĐHQG-HCM

TÓM TẮT: *Sau thành công của vi xử lý RISC 8-bit made-in-Vietnam SigmaK3 [1], chúng ta đã thiết kế và phát triển chip vi xử lý 8-bit thế hệ tiếp theo HN-07 với tốc độ cao hơn và thêm vào các đặc tính mới. Mục đích của bài báo này là mô tả những ưu điểm và những khía cạnh mới của chip vi xử lý HN-07. Kiến trúc của vi xử lý HN-07 dựa trên nền tảng chip SigmaK3 được thêm vào các đặc tính mới, như là kiến trúc pipeline 5-tầng, bộ điều khiển ngắt, nhiều ngoại vi bên được thêm vào, hoạt động ở tốc độ cao hơn và ổn định hơn. Kiến trúc cải tiến này làm cho HN-07 có thể được so sánh tương đương với các họ vi xử lý cùng loại khác như Intel 8051, Microchip PIC... Nhóm tác giả không chỉ thiết kế và mô tả phần cứng cho HN-07 ở giai đoạn front-end, mà còn thực hiện phần layout ở giai đoạn back-end.*

Từ khóa: microprocessor, RISC, computer architecture, pipeline.

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