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Original Research

Variable Pulse Density Modulation for a Buck-Type Three-Switch Current Source Rectifier

Thuong Phi Ngo, Nguyen Dinh Tuyen, Nam Quang Nguyen*

ABSTRACT

With flexible voltage adjustment without an intermediate DC/DC converter, short-circuit protection, self-starting, high reliability, and three-phase current source rectifiers (CSRs) are being widely used in high-power medium-voltage applications and low-power low-voltage applications. Modulation methods significantly affect the performance of CSRs and can be categorized into offline modulation methods, such as selective harmonic elimination/compensation pulse width modulation (SHE/SHC-PWM), and online modulation methods, such as space vector pulse width modulation (SV-PWM) and carrier-based pulse width modulation (CB-PWM). The SHE/SHC-PWM is popular in high-power medium-voltage applications that do not require a fast dynamic response and have a low switching frequency. Online modulations considerably improve the dynamic response and performance of the CSR; however, high computational power, such as digital signal processors (DSPs), is required at higher switching frequencies, leading to greater system complexity and cost. In this paper, an offline method based on variable pulse density modulation (VPDM) of power switches to synthesize sinusoidal input currents and control power transfer with pulse width modulation (PWM) is proposed. The proposed modulation is applicable to the three-switch buck-type VIENNA rectifier, showing the capability of improving the input current total harmonic distortion (THD) with respect to the SHE-PWM and is comparable to online modulations at a sufficiently high switching frequency. The simulation and experimental results basically prove the feasibility of the proposed modulation.

Key words: Pulse density modulation, Vlennar rectifier, buck-type rectifier, PFC rectifier

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INTRODUCTION

Traditional three-phase AC/DC converters, namely, diode rectifiers and thyristor-based rectifiers, have been widely used as the first stage in many power electronic configurations to provide unidirectional or bidirectional DC power in an uncontrolled or phase-controlled manner. With these configurations, the input power quality will be low; specifically, the input current total harmonic distortion (THD) will be high, the input power factor will be low, there will be high ripples on the DC output, low efficiency, and bulky AC and DC filters. On the other hand, power quality regulations on the user side are increasingly gaining attention with recent updates on related standards [1,2]. Transistor-based rectifiers have therefore been developed to overcome these weaknesses and are divided into two groups, voltage source rectifiers (VSRs) and current source rectifiers (SRs), according to the energy storage component on the DC side. VSRs have been thoroughly studied and greatly improved for widespread industrial application because of their suitability for many nonlinear controllers [3,4], simple structure, and low losses. However, in some voltage step-down applications requiring a wider input voltage range and limited output current in cases of output short circuiting, the CSR configuration (see Figure 1) is preferred to adding another DC/DC stage after the VSR.

Moreover, CSRs are widely used not only in medium-voltage high-power applications (with symmetric gate commutated thyristors or gate turn-off thyristors) due to their simple structure and short-circuit protection [5] but also in low-power systems such as motor speed control [6], induction heating [7], electric vehicle chargers [8], and telecommunication power supplies [9]. The modulation methods used in CSRs can be divided into two groups: offline and online. Among offline methods, selective harmonics elimination/selective harmonics compensation (SHE/SHC) pulse width modulation (PWM) [10–13] is often used for medium-voltage high-power applications; this method does not require a fast dynamic response and has a low switching frequency to reduce switching losses. The sinusoidal PWM [14,15], space vector PWM [16–18], and carrier-based PWM [19,20] are online methods. A typical CSR is a six-switch rectifier, as illustrated in Figure 1, in which unidirectional switches can be im-

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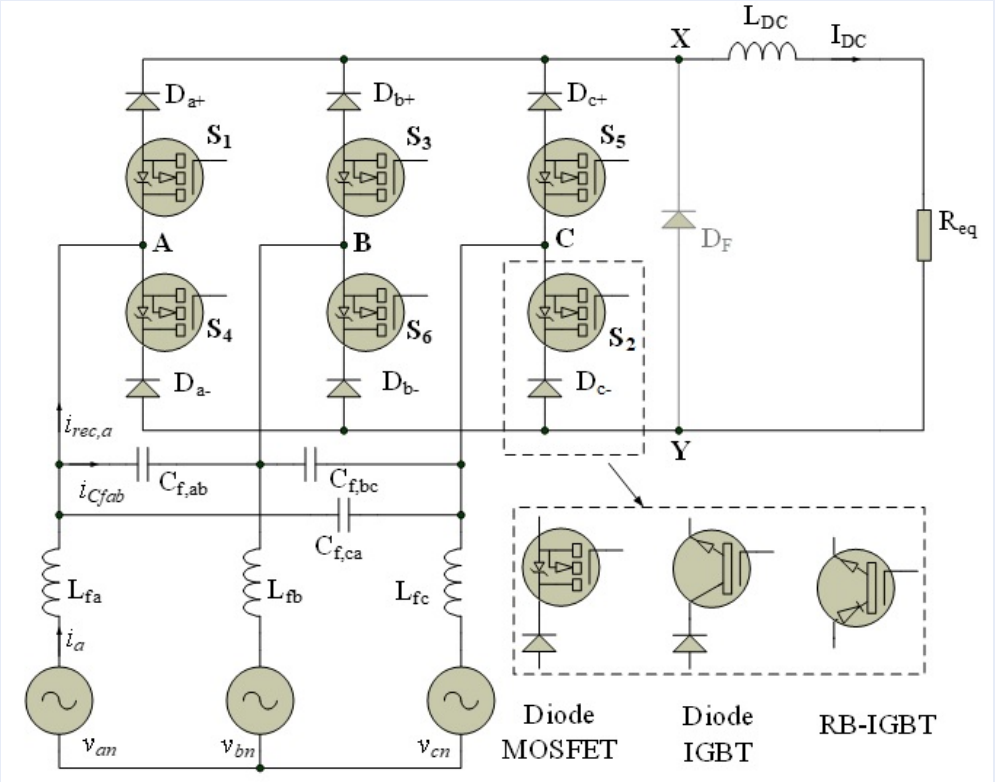


Figure 1: Three-phase six-switch current source rectifier

plemented with reverse blocking IGBTs (RB-IGBTs) or diodes in series with MOSFETs or IGBTs. Online modulations could significantly improve the dynamic response and performance of CSRs but require much greater computational power from digital controllers (microcontrollers or digital signal processors). With the growth of fast switching devices, such as SiC and GaN transistors, the computational power required for implementing faster switching frequencies (150 kHz and above) and complicated control algorithms will impose serious challenges on digital controllers or even field programmable gate arrays (FPGAs), leading to significant obstacles in designing converters with online algorithms[21].

The number of active switches in the six-switch rectifier can be reduced with the three-switch rectifier (illustrated in Figure 2a), as proposed for the first time in[22]; applying an offline PWM method on GTOs in[23]; and space vector PWM (SV-PWM) with a switching frequency below 35 kHz in[24–31], reaching an efficiency of 95.1%, as reported in[26]; and an input current THD of 6.9% for an open loop SV-PWM[25]. Carrier-based PWM can also be used for this topology with a switching frequency below 10 kHz, achieving an input current THD below 5% in simulations[32,33], and at 7.3% in experiments[34]. Similar simulated input current THD results have also been reported for sine PWM at 30 kHz[14], 20 kHz[35] and 10 kHz[15].

One of the main objectives of the above studies was to improve modulation methods to achieve an input current THD below 5% for all three phases, as standardized in[12]; however, the switching frequency is normally less than 35 kHz due to efficiency degradation at higher frequencies[18]. An offline variable pulse density modulator (VPDM) specifically designed for high switching frequency, aimed at a unity power factor and low input current THD, has been proposed for the three-switch current source rectifier (3SWCSR) and will be presented in this paper. The simulation results confirmed the feasibility of the proposed modulation algorithm with an input current THD of 8.6% at a 38.4 kHz switching frequency and 4.3% at 174 kHz. The experimental results at a 38.4 kHz switching frequency also confirmed the proposed solution. Next, a comparison between the VPDM and space vector PWM (SVPWM) is presented, followed by simulation and experimental results.

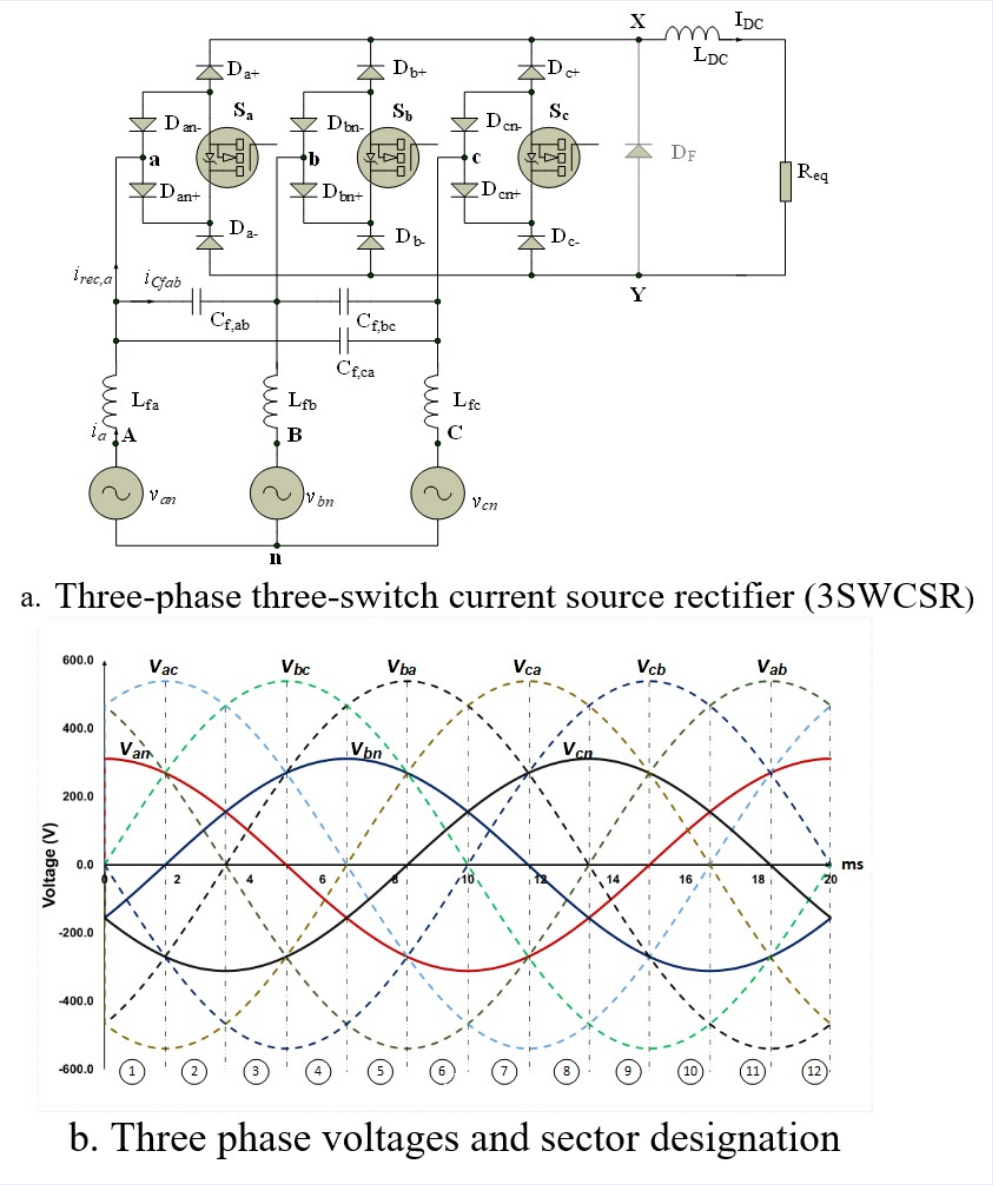


Figure 2: Three-phase three switch current source rectifier and sector designation

VARIABLE PULSE DENSITY MODULATION FOR ACTIVE RECTIFIERS

Assuming a balanced three-phase power supply, with the instantaneous phase voltages described in (1) (in which U_0 [V] is the phase voltage magnitude and ω_i [rad/s] is the angular frequency), is connected to the 3SWCSR, the input voltage sectors can be designated as shown in Figure 2b. The following analysis will be performed for sector 1 ($v_{an} > 0 > v_{bn} > v_{cn}$) and can be performed in a similar manner for other sectors.

$$v_{iph}(t) = \begin{bmatrix} v_{an}(t) \\ v_{bn}(t) \\ v_{cn}(t) \end{bmatrix} = U_0 \begin{bmatrix} \cos(\omega_i t) \\ \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ \cos\left(\omega_i t + \frac{2\pi}{3}\right) \end{bmatrix}$$

On-$_{time,\ skip}$ (k = a, b, c) ($S_k = 0$ means the corresponding switch is turned off, $S_k = 1$ indicates that the corresponding switch is in an on-state) for a switching state j = ($S_a S_b S_c$) in the online SV-PWM, and the proposed VPDM will be implemented on the basis of the following assumptions[29] for simplicity:

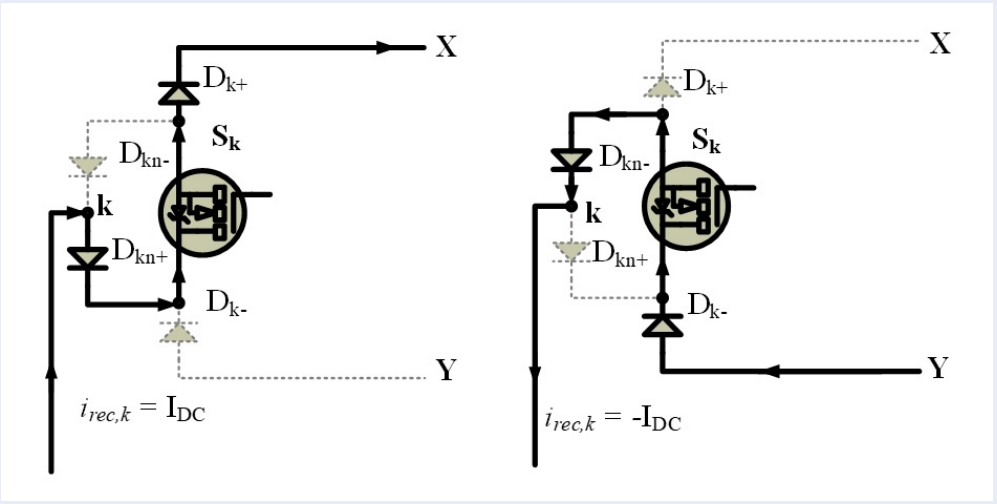


Figure 3: Current flow and ON switch status

- The voltages on the input filter capacitors ($C_{f,ab}$, $C_{f,bc}$, $C_{f,ca}$) of the 3SWCSR are sinusoidal and in phase with the main phase voltages. Hence, the voltage drops on the filter inductors ($L_{f,a}$, $L_{f,b}$, and $L_{f,c}$) can be neglected.
- The main currents (i_a, i_b, i_c) are assumed to be equal to the fundamental component of the rectifier input currents ($i_{rec(1),a}$, $i_{rec(1),b}$, $i_{rec(1),c}$); therefore, the reactive currents due to the filter capacitors are also neglected.
- With a sufficiently large DC output inductor, the current through the output inductor I_{DC} is assumed to be constant, meaning that the high-frequency ripple due to the switching operation is neglected.
- With the above assumptions, the SV-PWM for 3SWCSR will be described next for comparison with the proposed VPDM later on the same topology.

A. Online Space Vector Pulse Width Modulation of Input Currents

For the 3SWCSR in Figure 2a, S_k in the on-state (S_k = 1) connects node k to one branch of the rectifier via a block diode D_{kn+} (or D_{kn-}) corresponding to the positive (or negative) current from the mains to the rectifier. It is possible to identify current paths for all switching states. Depending on whether the current direction between the mains and the rectifier is positive ($i_{rec,k} = I_{DC}$) or negative ($i_{rec,k} = -I_{DC}$), a mains phase (a, b, c) will be connected to node X (or node Y), as in Figure 3, for the same switching state; alternatively, no output nodes (indicated by node O) will be connected to the mains phase. For example, if state j = (101), as illustrated in Figure 4a, S_a and S_c are turned on, allowing currents $i_{rec,a} = I_{DC}$ (a connected to X) and $i_{rec,c} = -I_{DC}$ (c connected to Y) to flow between phase A and phase C, forming a current space vector $\vec{i}_{ac}$ [XOY]. All possible switching states are shown in Figure 4 for sector 1. All the switching states and corresponding current space vectors are shown in Table 1 and illustrated in Figure 5. There are six active vectors and 4 zero vectors. Any active vector can be implemented in the (111) state, and the current flow will be determined by instantaneous phase voltages, similar to a traditional three-phase diode bridge rectifier. For this modulation, slow switching devices, such as BJTs or IGBTs, can be used. However, it would be difficult to apply soft switching techniques due to the one-way current flow through these devices. This should limit the switching frequency to below 100 kHz [36] unless fast switching devices, such as Si MOSFETs or SiC/GaN transistors, are used.

Online SV-PWM at switching frequencies below 35 kHz was fully developed with high performance in [24–34], in which a particular switching state sequence was proposed to reduce the input current THD due to glitching at sector boundaries in [29]. In this modulation, each sequence includes two active states and one free-wheeling state, which are symmetrically arranged. For example, in sector 1, the symmetric sequence (101)-(110)-(010)-(110)-(101) is applied, where j = ($S_aS_bS_c$) indicates a combination of

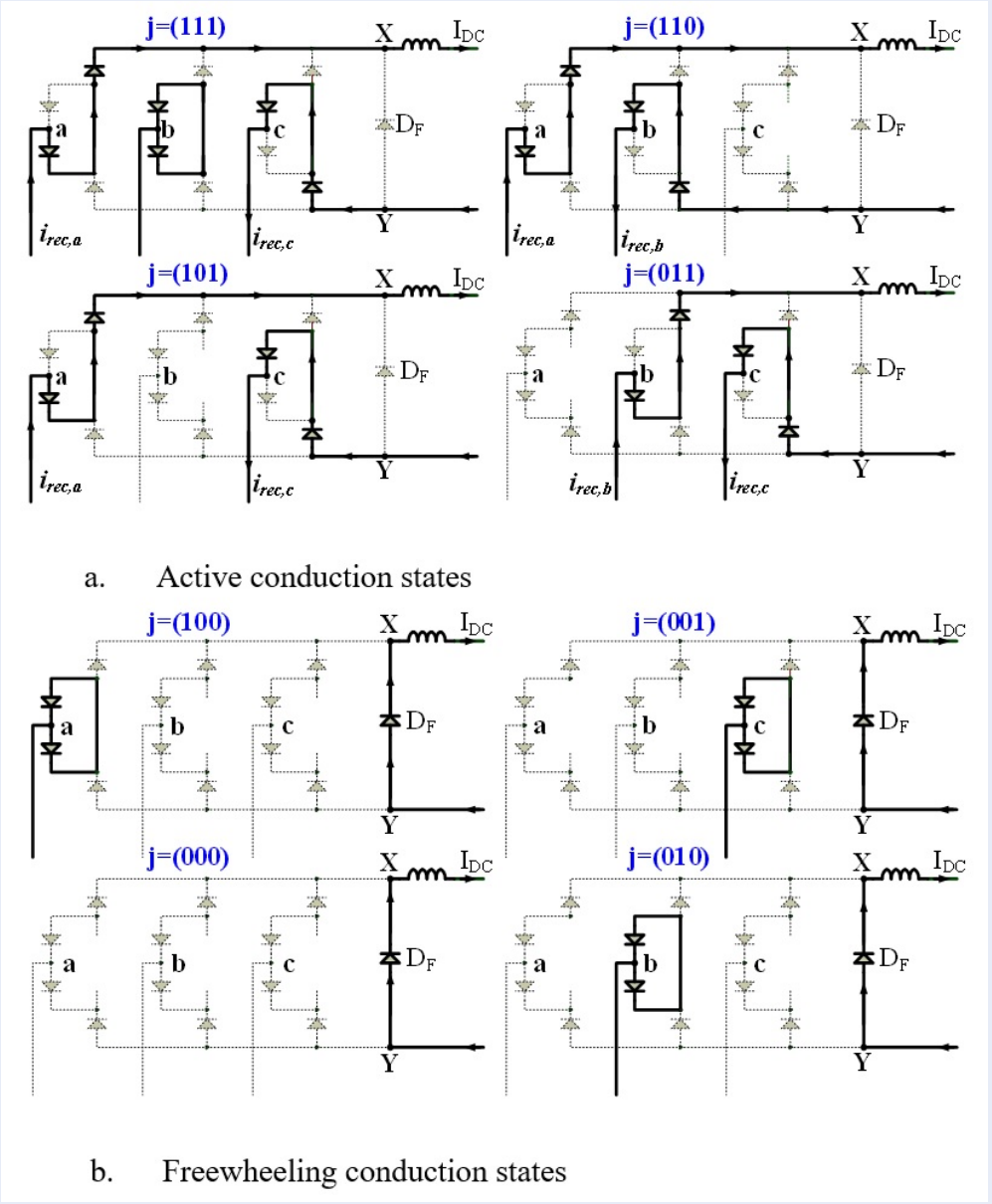


Figure 4: 3SWCSR conduction states in sector 1 ($v_{an} > 0 > v_{bn} > v_{cn}$)

the three switches, state '1' means the corresponding switch is turned on, and state '0' indicates that the corresponding switch is in an off-state. The relative on-times for switches in active and free-wheeling states are determined as in (2) - (5) [29], in which $M = I_0/I_{DC}$ is the modulation index, I_0 is the magnitude of the input phase currents, I_{DC} is the DC current, and v_{an}, v_{bn}, and v_{cn} are instantaneous input phase voltages[25].

$$\delta_{1.ac} = -M\frac{v_{cn}}{U_0}$$

$$\delta_{1.ab} = -M\frac{v_{bn}}{U_0}$$

$$\delta_{FW} = 1 - M\frac{v_{an}}{U_0}$$

$$\vec{i}_{ref}(t) = \delta_{1.ac}\,\vec{i}_{ac[XOY]} + \delta_{1.ab}\,\vec{i}_{ab[XYO]}$$

From equations (2) - (5), to implement the SV-PWM, the controller must continuously sample the instantaneous input phase voltages before each switching cycle and calculate all the relative on-time voltages

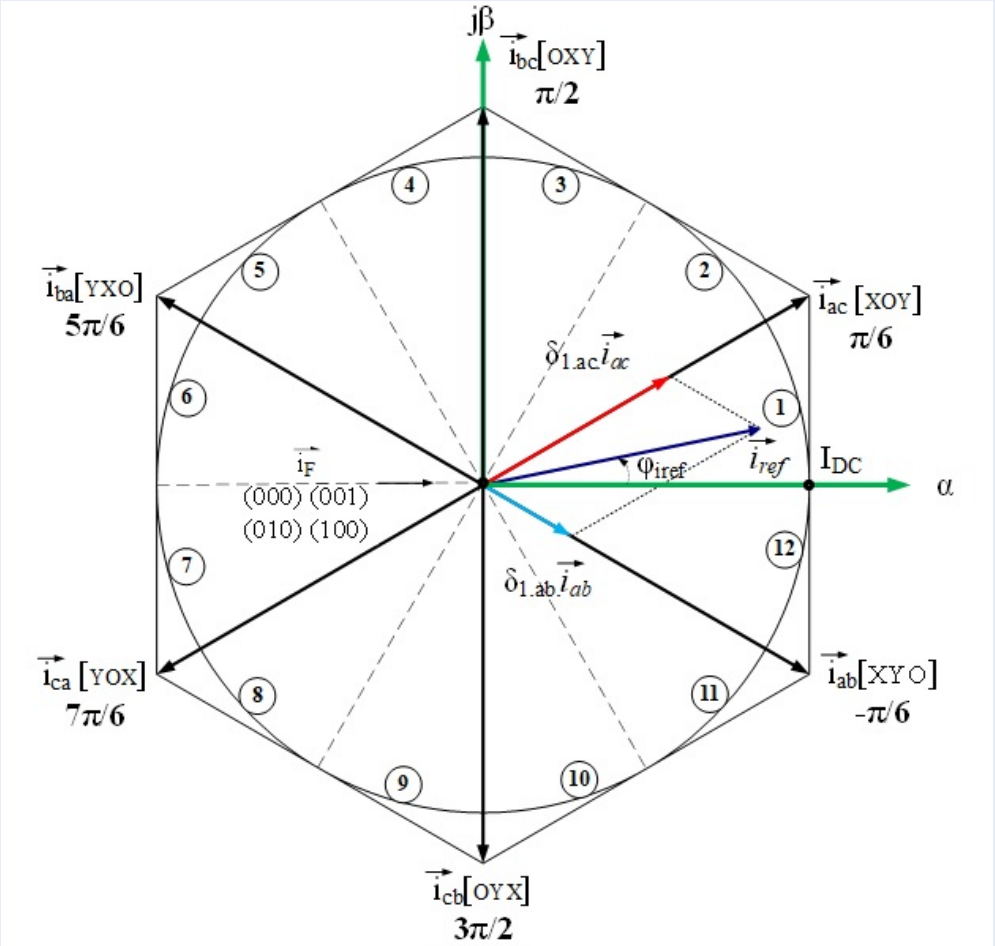
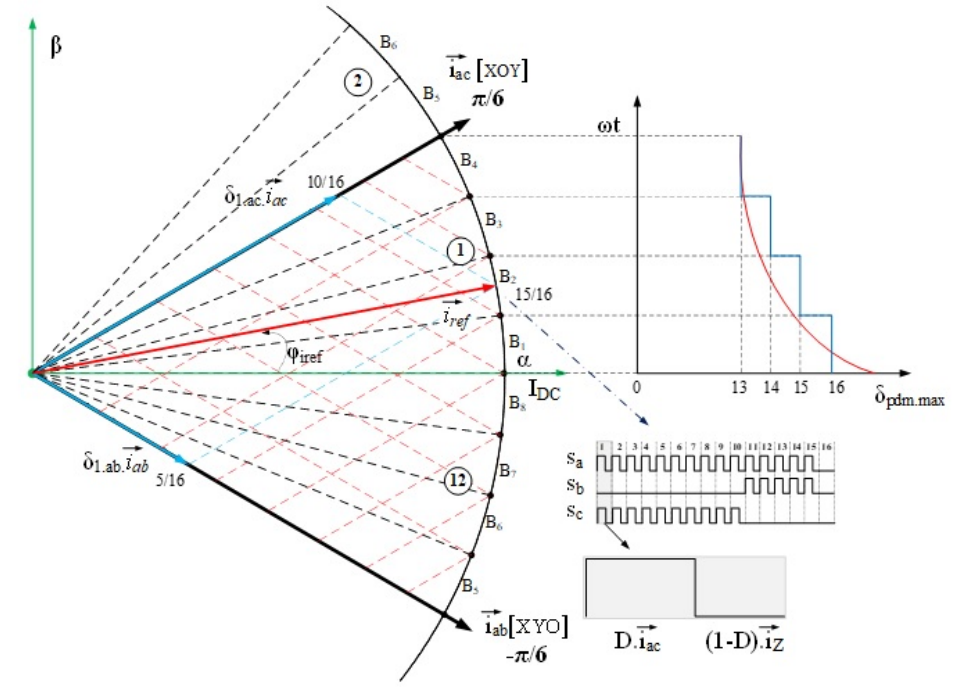


Figure 5: Current space vector

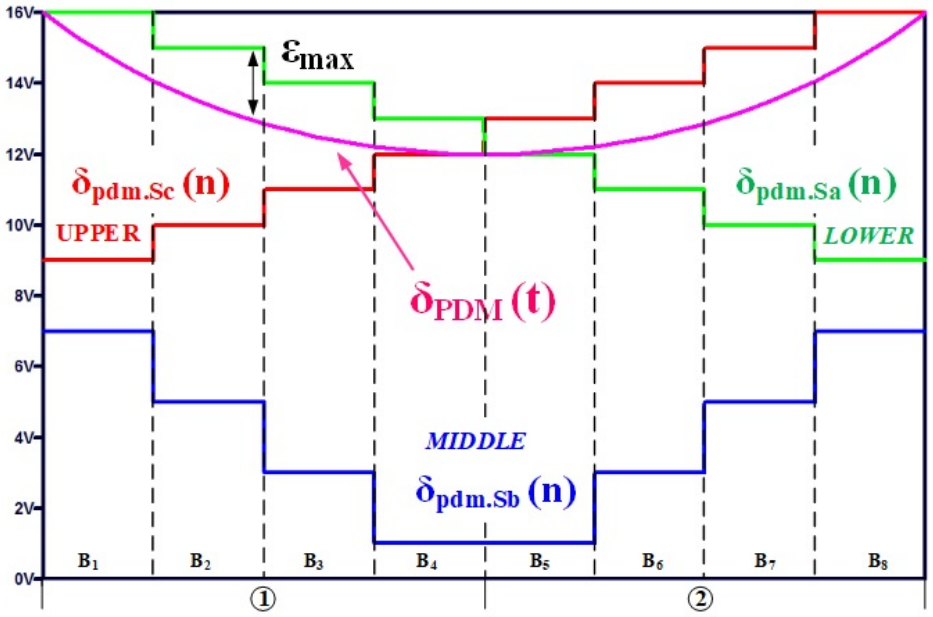
using trigonometric expressions. For higher switching frequencies, the available time for calculations will be shorter, and some predictive algorithms might be needed or the switching frequency could not increase much. This problem can be solved with offline modulations, such as pulse density modulation (PDM), in which relative on-times can be predetermined and saved in lookup tables. PDM was first applied to VSR in 1992[37], in which an active-voltage clamped resonant DC link (ACRDCL) was used to divide voltage vectors in each sampling period into four blocks to reduce errors introduced by selecting the closest vector in the SV-PWM. However, calculations on the d-q reference frame still need to be performed on the DSP; at the same time, a predictive algorithm is needed for current estimation on the ACRDCL due to calculating limitations of the DSP. In[38], a PDM algorithm was proposed for a three-phase to single-phase matrix converter in induction heating applications with zero-voltage switching (ZVS) on bidirectional switches owing to the high-frequency AC load current to synthesize sinusoidal input currents at a unity power factor. In addition to those two studies, there have been no publications on the application of the PDM to current source rectifiers. The fundamentals of PDM control will be described next.

B. Variable Pulse Density Modulation (VPDM)

In this section, a VPDM algorithm is proposed for a hard-switching 3SWCSR at frequencies less than 50 kHz to simplify the implementation and analysis, as illustrated in Figure 6 for input sector 1. Each sector is divided into four equal blocks, and each block includes sixteen switching cycles. For an exact 50 Hz main cycle, a perfect fit should require 768 switching cycles, leading to a 38.4 kHz switching frequency and no line synchronization. An offline pulse distri-



a. VPDM in sector 1



b. PDM quantization

Figure 6: VPDM method in sector 1

Table 1: Current Space Vectors

Vector	Switches			Input currents			$\lvert \vec{i}_{\alpha\beta} \rvert < \varphi_i$	V_{dc}
	S_a	S_b	S_c	$i_{rec,a}$	$i_{rec,b}$	$i_{rec,c}$		
$\vec{i}_{ab}$ [XOY]	1	0	1	I_{DC}	0	- I_{DC}	$\frac{2}{\sqrt{3}} I_{DC} < \frac{\pi}{6}$	v_{an} - v_{cn}
	1	1	1					
$\vec{i}_{bc}$ [OXY]	0	1	1	0	I_{DC}	- I_{DC}	$\frac{2}{\sqrt{3}} I_{DC} < \frac{\pi}{2}$	v_{bn} - v_{cn}
	1	1	1					
$\vec{i}_{ba}$ [YXO]	1	1	0	- I_{DC}	I_{DC}	0	$\frac{2}{\sqrt{3}} I_{DC} < \frac{5\pi}{6}$	vbn - v_{an}
	1	1	1					
$\vec{i}_{ca}$ [YOX]	1	0	1	- I_{DC}	0	I_{DC}	$\frac{2}{\sqrt{3}} I_{DC} < \frac{7\pi}{6}$	v_{cn} - v_{an}
	1	1	1					
$\vec{i}_{cb}$ [OYX]	0	1	1	0	- I_{DC}	I_{DC}	$\frac{2}{\sqrt{3}} I_{DC} < \frac{3\pi}{2}$	v_{cn} - v_{bn}
	1	1	1					
$\vec{i}_{ab}$ [XYO]	1	1	0	I_{DC}	- I_{DC}	0	$\frac{2}{\sqrt{3}} I_{DC} < -\frac{\pi}{6}$	v_{an} - v_{bn}
	1	1	1					
	1	0	0	0	0	0	0	0
	0	1	0					
	0	0	1					
	0	0	0					

bution pattern can be used to synthesize three-phase input currents, while power transfer can be regulated by pulse width modulation.

Considering a balanced three-wire three-phase system, the distribution pattern must ensure that the algebraic sum of the instantaneous input currents is zero at all times, meaning that the current will exit one input phase to spread into the other two phases or that two input phase currents will flow into the remaining phase. For example, considering sector 1 ($v_{an} > 0 > v_{bn} > v_{cn}$), the current going out of phase A should be equal to the sum of the currents going into phase B and phase C ($I_A = I_B + I_C$), and power is being transferred from V_{AB} and V_{AC} sources to the load, with S_b or S_c being used to connect node b or node c to node Y, while S_a is used to connect node a to node X. In the next sector, sector 2, a similar condition exists with two available positive voltage sources of V_{AC} and V_{BC}, in which S_a or S_b is used to connect node a or node b to node X, while S_c is used to connect node c to node Y. Instantaneous current going into phase C equals the sum of the currents going out of phase A and phase B ($I_C = I_A + I_B$). Table 2 summarizes all the valid switching states for the VPDM algorithm in all 12 input sectors. Let $\delta_{pdm.Sk}(n)$ be the pulse density distribution function of switch S_k (k = a, b, c), in which each pulse has a width of D, as illustrated in Figure 6a; switch S_a has a density of 15/16 at the block under consideration, while the instantaneous phase currents can be presented as in (6) as functions of these pulse density distribution functions (n is the block index).

$$i_{iph}(n) = \begin{bmatrix} i_{rec,a}(n) \\ i_{rec,b}(n) \\ i_{rec,c}(n) \end{bmatrix} = I_{DC}.D \begin{bmatrix} \delta_{pdm.Sa}(n) \\ i_{pdm.Sb}(n) \\ i_{pdm.Sc}(n) \end{bmatrix}$$

In each sector, the magnitude of the maximum instantaneous current in (6) should be proportional to the magnitude of the highest absolute instantaneous line-

Table 2: Switching states and current equations

Interval/Sector		Switching States		Current equation	Source
		X	Y		
I	1	S_{AX}	S_{BY}/S_{CY}	$I_A = I_B + I_C$	v_{ab}, v_{ac}
	2	S_{AX}/S_{BX}	S_{CY}	$I_C = I_A + I_B$	v_{bc}, v_{ac}
II	3	S_{BX}/S_{AX}	S_{CY}	$I_C = I_A + I_B$	v_{bc}, v_{ac}
	4	S_{BX}	S_{AY}/S_{CY}	$I_B = I_A + I_C$	v_{bc}, v_{ba}
III	5	S_{BX}	S_{CY}/S_{AY}	$I_B = I_A + I_C$	v_{bc}, v_{ba}
	6	S_{BX}/S_{CX}	S_{AY}	$I_A = I_B + I_C$	v_{ba}, v_{ca}
IV	7	S_{CX}/S_{BX}	S_{AY}	$IA = I_B + I_C$	v_{ba}, v_{ca}
	8	S_{CX}	S_{BY}/S_{AY}	$I_C = I_A + I_B$	v_{ca}, v_{cb}
V	9	S_{CX}	SAY/S_{BY}	$I_C = I_A + I_B$	v_{ca}, v_{cb}
	10	S_{CX}/S_{AX}	S_{BY}	$I_B = I_A + I_C$	v_{cb}, v_{ab}
VI	11	S_{AX}/S_{CX}	S_{BY}	$I_B = I_A + I_C$	v_{cb}, v_{ab}
	12	S_{AX}	S_{CY}/S_{BY}	$IA = I_B + I_C$	v_{ab}, v_{ac}

to-line voltage, with the expression of this instantaneous line-to-line voltage as (7) for sector 1.

$$v_{LL} = \sqrt{3}U_0 \cos\left(\omega_i t - \frac{\pi}{6}\right)$$
$$0 \le \omega_i t \le \frac{\pi}{6}$$

The highest absolute instantaneous line-to-line voltage is created from two (out of three) input phase voltages and provides power to the two-wire load via the DC link voltage. Due to the symmetry of the three-phase input system, the role of the input phases can be swapped in the input sectors to form the six-pulse rectified voltage, as shown in Figure 2b. If there are enough blocks in each sector, it can be assumed that in one block, the instantaneous line-to-line voltage is practically constant [38]. Let $\delta_{PDM}(t)$ be the pulse density of the switches used to create the line-to-line voltage in that block; then, the average line-to-line voltage in the block (VPDM) will be proportional to this pulse density, as in (8):

$$V_{PDM} = v_{LL}(t).\delta_{PDM}(t)$$

From (6-8), we can see that the VPDM is proportional to $\cos\left(\omega_i t - \frac{\pi}{6}\right)$, as in (9):

$$V_{PDM} \propto \cos\left(\omega_i t - \frac{\pi}{6}\right)$$

On the other hand, for sinusoidal input phase currents, the total three-phase power transferred from the source to the load should be constant; therefore, the pulse density functions must be regulated so that the average line-to-line voltage VPDM is constant. Because the transferred power is proportional to the square of the available voltage for a given pulse density, the output power can be maintained constant if the pulse density is implemented as in (10) [38]:

$$\delta_{PDM}(t) = \frac{\cos^2\left(\frac{\pi}{6}\right)}{\cos^2\left(\omega_i t - \frac{\pi}{6}\right)},\ 0 \le \omega_i t \le \frac{\pi}{6}$$

The function $\delta_{PDM}(t)$ is quantized (for a digital implementation of the algorithm), plotted for the number of blocks of the implemented algorithm in Figure 6b, and applied for the phase with the highest absolute instantaneous voltage; for example, in sector 1, it is phase A, and the density of the other two input phases can be determined by (6) and (11).

$$\delta_{PDM}(t) = \max_{1\le n\le 4}\{\delta_{pdm.Sa}(n), \delta_{pdm.Sb}(n), \delta_{pdm.Sc}(n)\}$$

In Figure 6b, the exact time function of pulse density δ_{PDM}(t) for the VPDM algorithm is depicted, together with quantized pulse density functions for the input phases $\delta_{pdm.Sc}(n)$ (UPPER), $\delta_{pdm.Sa}(n)$ (LOWER) and $\delta_{pdm.Sb}(n)$ (MIDDLE). To implement the VPDM algorithm, PDM patterns for the most positive phase (UPPER) and the most negative phase (LOWER) are taken from a preset lookup table (for example, in the FPGA), and the last PDM for the third phase should be determined from a logical combination of the first two PDM patterns to fulfill the requirement of $I_A + I_B + I_C = 0$ in a three-wire three-phase system.

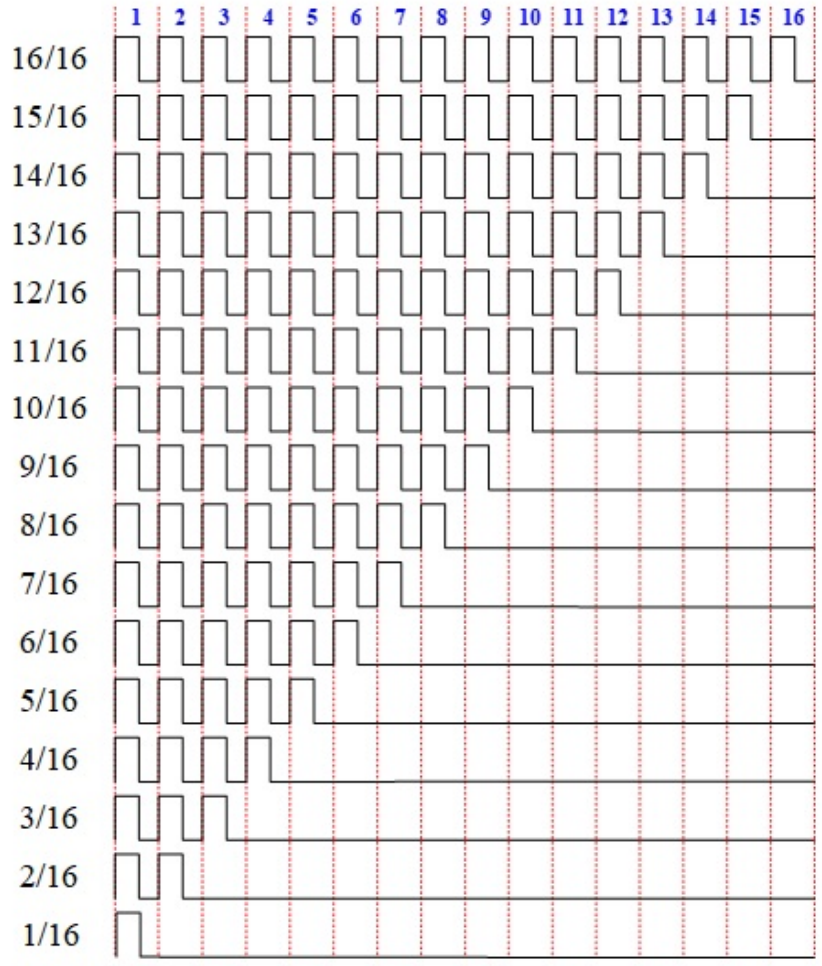


Figure 7: Noninterlacing PDM pattern

For line frequency synchronization, the number of PDM blocks and the switching frequency should satisfy (12), in which f_s is the switching frequency [Hz]; f_{grid} is the line frequency [Hz]; n_B is the PDM block length (number of switching cycles per PDM block) [pulse/block]; and B_B is the number of blocks per sector [block/sector]. The PDM block length n_B should be large to ensure good magnitude resolution (16, 32, or 48 or more). However, this approach would reduce the temporal resolution. Furthermore, a large number of PDM blocks Bb (corresponding to a small PDM block length) are required to ensure effective line frequency synchronization, and the details of the proposed solution for VPDM are described in section IV of this paper.

$$f_s = f_{grid}\,[Hz] \times n_B\,[pulse/block] \times \\ \times 6B_B\,[block/sector]$$

A simple PDM pattern is drawn in Figure 7, which is applied to the reference current vector, as illustrated in Figure 6a, in which the Sa, Sb, and S_c switches have pulse densities of 15/16, 5/16, and 10/16, respectively. Due to quantization error, it can be predicted that at several positions in each sector (e_{max} in Figure 6b), there could be some current glitches. For a given pulse density, the distribution pattern in a block can also affect the input waveform, similar to the switching sequence of active and zero vectors in SV-PWM. Two other PDM patterns can also be used for 16-pulse blocks, as shown in Figure 8, where the hybrid pattern drawn in Figure 8a is a combination of the noninterlacing pattern shown in Figure 7 and the interlacing pattern depicted in Figure 8b. The noninterlacing PDM pattern provides the best overall efficiency among the three VPDM strategies with the

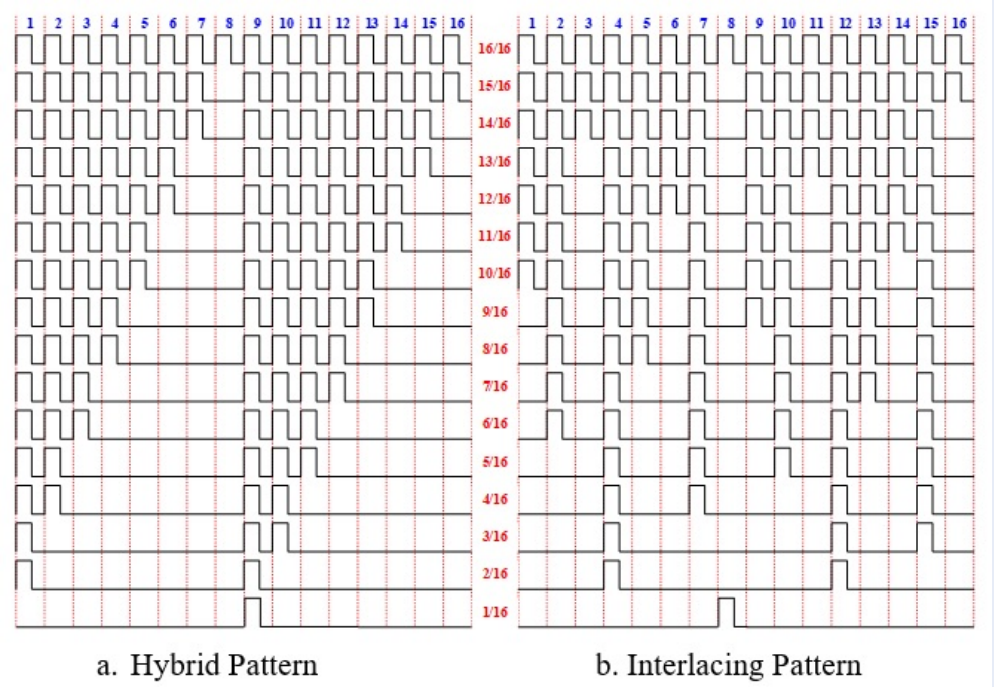


Figure 8: Hybrid and interlacing PDM pattern

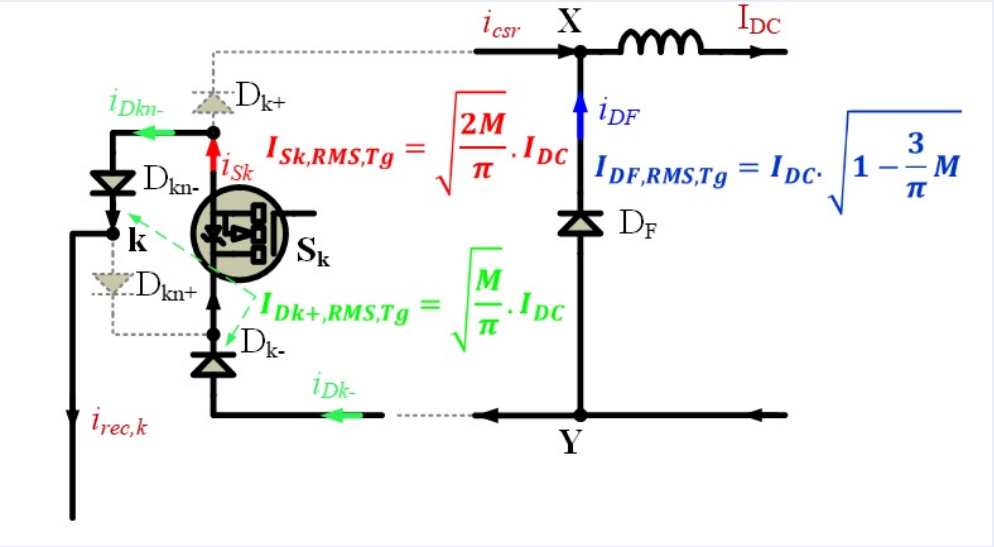


Figure 9: Current stress in semiconductor devices of 3SWCSR

same PDM varying algorithm, while the interlacing pattern gives a better power factor. Next, the simulation results of SV-PWM and VPDM on the 3SWCSR will be presented, and a performance comparison and evaluation will be performed.

SIMULATION RESULTS AND DISCUSSION

To verify the feasibility and evaluate the AC input and DC output quality of a 3SWCSR model with the proposed VPDM algorithm, a 5 kW, 38.4 kHz rectifier, with the design specifications given in Table 3, is simulated and evaluated with reference to standards [1,2] in the input current harmonics. Furthermore, key parameters for the applied VPDM algorithm are also summarized, together with AC input filter parameters and DC output filter parameters calculated according to the procedure proposed in [39,40], with adjustments for the proposed VPDM. In addition, SV-PWM is simulated for comparison using the same hardware structure and ratings (the 3SWCSR) and parameters presented in [29]. Next, the voltage and current stresses on the semiconductor components are calculated to fulfill the design parameters in Table 3, for component selection in the simulations, and in the demonstration prototype.

A. Semiconductor Voltage and Current Stresses

In this section, the stresses on semiconductor components are calculated according to the operating parameters of the converter, which is important in system design and provides a basis for selecting suitable components to verify the feasibility of the algorithm via simulation and experimentation. The voltage stress can be quickly determined from the magnitude line-to-line voltage of the three-phase system under the maximum allowable voltage deviation (10% in Vietnam), as in (13). However, a voltage headroom of 50% should be used as the absolute voltage on the component to account for transient glitches and harmonic voltages.

$$U_{0,LL,max} = \sqrt{6}U_{rms}\left(1+\triangle u_{cp}\%\right) = \sqrt{6}.220.(1+10\%) = 593\ V$$

Current stresses are harder to determine because they are related to the modulation algorithm being used, the switching frequency, and other conditions in the source and load. RMS values are necessary to determine the current rating and power losses of the component in the design procedure. In VPDM, the current waveform depends on the number of blocks per sector, the block length, the PDM pattern, and the pulse width. All these parameters are selected to implement the pulse density curve (10) as closely as possible in each sector, and the analysis of the current waveform is not considered in this paper. However, it can be assumed that with a large enough number of blocks, sinusoidal input currents can be implemented, and the power transferred to the load is the same for both the SV-PWM and VPDM. Therefore, the current stresses are determined by calculations deduced for the SV-PWM as a reference, and the discrepancy in the simulated current stresses for both algorithms is evaluated.

The RMS value of the input current is now considered to determine the current stresses on diodes and switches. Due to the symmetry of the three-phase system, it is sufficient to study only one input phase. For example, the local RMS value of the phase A input current over a switching cycle can be determined from the instantaneous i_a current (14), giving the square RMS value over a switching cycle T_s in (15). The global square RMS value (over a mains cycle T_g) of the phase A input current is then given in (16).

$$i^2_{rec,a,RMS,Ts} = \begin{cases} (\delta_{1.ac}+\delta_{1.ab}).I^2_{DC}\ Interval\ I \\ \delta_{2.ac}.I^2_{DC}\ Interval\ II \\ \delta_{6.ac}.I^2_{DC}\ Interval\ VI \end{cases}$$

$$i^2_{rec,a,RMS,Interval} \approx \frac{1}{Tg/6}\int^{\square}_{Interval} i^2_{rec,a,RMS,Ts}dt$$

$$i^2_{rec,a,RMS,Tg} = \frac{2M}{\pi}.I^2_{DC}$$

By examining the current waveforms on the phase A leg, the RMS values of the currents in the corresponding switch S_k and diodes can be estimated by (17) - (19) and are given in Figure 9. The analytical and simulated current stresses on these components for both the SV-PWM and VPDM simulations are compared in Table 4. The discrepancies between the analytical and SV-PWM simulation results are due to the omission of harmonics and current glitches in the above analysis. Therefore, analytical current stresses can be used to select semiconductor components for 3SWCSR. Next, simulations for evaluating the performance of the proposed VPDM algorithm are described.

$$I_{Sk,RMS,Tg} = \sqrt{\frac{2M}{\pi}}.I_{DC}$$

$$I_{Dk,RMS,Tg} = I_{Dkn,RMS,Tg} = \sqrt{\frac{M}{\pi}}.I_{DC}$$

$$I_{DF,RMS,Tg} = \sqrt{1-\frac{3M}{\pi}}.I_{DC}$$

Table 3: Simulation Parameters

Parameter		Value	
Power Supply		3 phases, 220 V/380 V – 50 Hz	
Rated Power P_n		5 kW	
PF		> 0.9	
THD_i		< 5%	
AC Filter	C_f	1.5 μF	
	L_f	5 mH	
	R_{dump}	45 Ω	
DC Filter	C_{dc}	1000 μF	
	L_{dc}	2 mH	
VPDM		B_B	8 Block
		n_B	16 pulse
		f_s	38.4 kHz

Table 4: Comparison Of RMS Current Stresses In Simulations AndCalculations

Current	Analytics [A]	SIMULATION SV-PWM (M = 0.85)		SIMULATION PDM (D = 0.95)	
		Value [A]	Deviation [%]	Value [A]	Deviation [%]
$I_{Sk,RMS}$	9.3068	9.3946	0.9	9.7365	4.6
$I_{Dk,RMS}$	6.5809	6.6545	1.1	6.8986	4.8
$I_{DF,RMS}$	5.318	4.9385	7.7	4.5015	15.4
I_{DC}	12.5	12.578		12.544	

B. Simulation Results and Discussions

To evaluate the performance of the proposed VPDM algorithm for the 3SWCSR scenario, a simulation model with a 5 kW rating was built, as shown in Figure 10, in which the load is a resistor in parallel with the output capacitor C_{dc} and the CSR is acting as a variable DC voltage source. The control scheme is shown in Figure 10b, where a 38.4 kHz PWM signal is created by comparing the demand DC voltage and the real DC voltage. PWM pulses are distributed to $S_aS_bS_c$ according to the preset VPDM pulse mapping for the corresponding input sector and are detected by a zero-crossing detector (ZCD). Both SV-PWM (at a 12 kHz switching frequency) and VPDM (at a 38.4 kHz switching frequency) will be simulated.

In Figure 11, the input current i_{abc}, phase A input voltage V_{an}, and DC output voltage VDC waveforms are presented for both the SV-PWM and VPDM algorithms. Both algorithms create a high power factor of 0.99 and a low ripple DC output voltage at the rated power. The SV-PWM can provide a high-quality input current with a THDi of 3.3%, while the VPDM produces a higher harmonic content with a THDi of 8.6% (the THD is calculated for harmonics up to the 30th). An FFT analysis was performed on the input current waveform created by the VPDM, revealing the good filtering effect of the input filter; however, high magnitudes (over 5%) occurred at the 23rd and 25th harmonics, leading to high THDi. The higher order structure of the CSR with respect to VSR could be the reason, due to the possibility of resonances among the input filter and output filter components, leading to some high harmonics. Furthermore, the selection and distribution of PWM pulses in VPDM should affect the current THD but will not be considered in this paper. The relative power losses of VPDM (93.28% efficiency) and SVPWM (95.62% efficiency) were analyzed, and the power losses on the filters were significantly different, as shown in Figure 12b. The power losses on filters (and other supporting components) in the VPDM are five times greater than those in the SVPWM due to the addition of the R_{dump} and ESRs

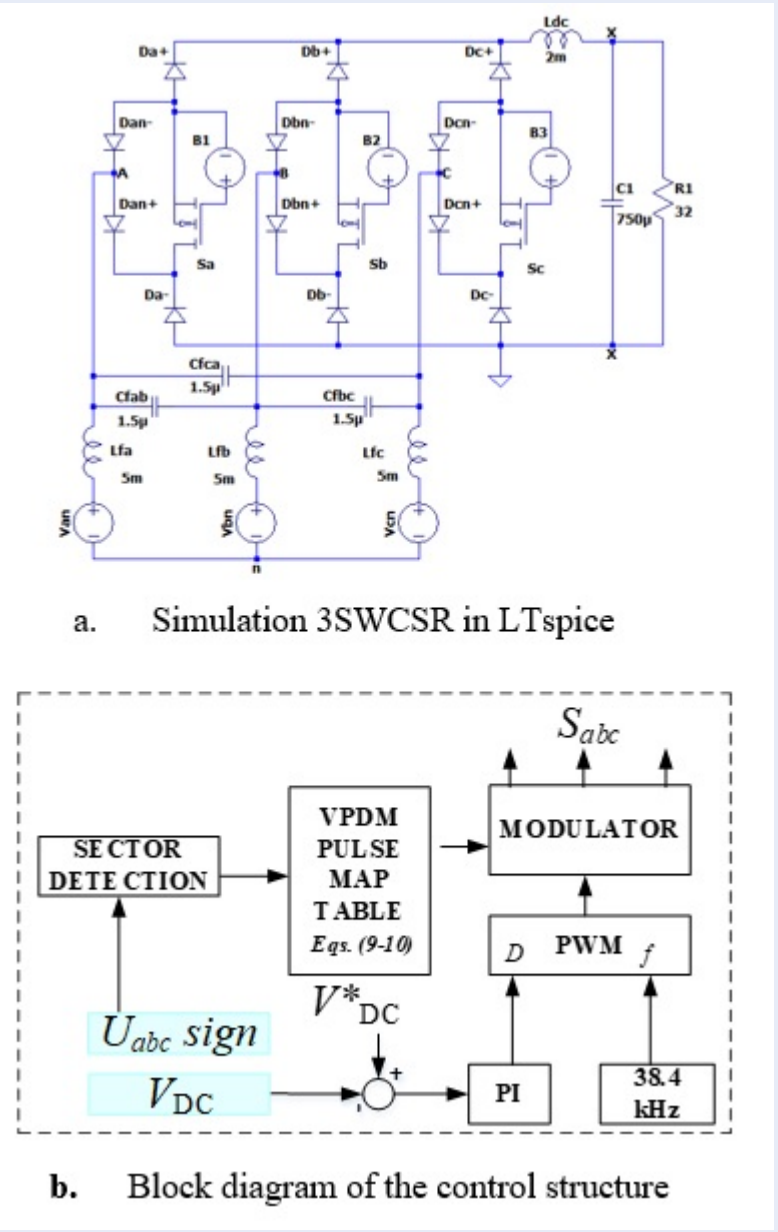


Figure 10: Simulation and control scheme

of inductors and capacitors needed to achieve low harmonic distortion in the VPDM. This can be improved by using different PDM patterns or higher switching frequencies.

To demonstrate the effect of the switching frequency in VPDM, a simulation with a 174 kHz switching frequency, Bb = 36, and n_b = 16 was performed with the resulting waveforms shown in Figure 13.

In Figure 13, the simulated input current THD is reduced from 8.6% at a 38.4 kHz switching frequency to 4.3% at 174 kHz. The error ε_{MAX} would not considerably affect the input current waveform because at a higher switching frequency, the VPDM should have a higher resolution to closely approximate the pulse density given in (9). On the other hand, current glitches at sector boundaries are still significant, as shown in Figure 12, similar to online algorithms such as the SV-PWM in [24–31].

Next, line frequency synchronization and PDM patterns are discussed, followed by a description of the experiments on a prototype using MOSFET with a 38.4 kHz switching frequency.

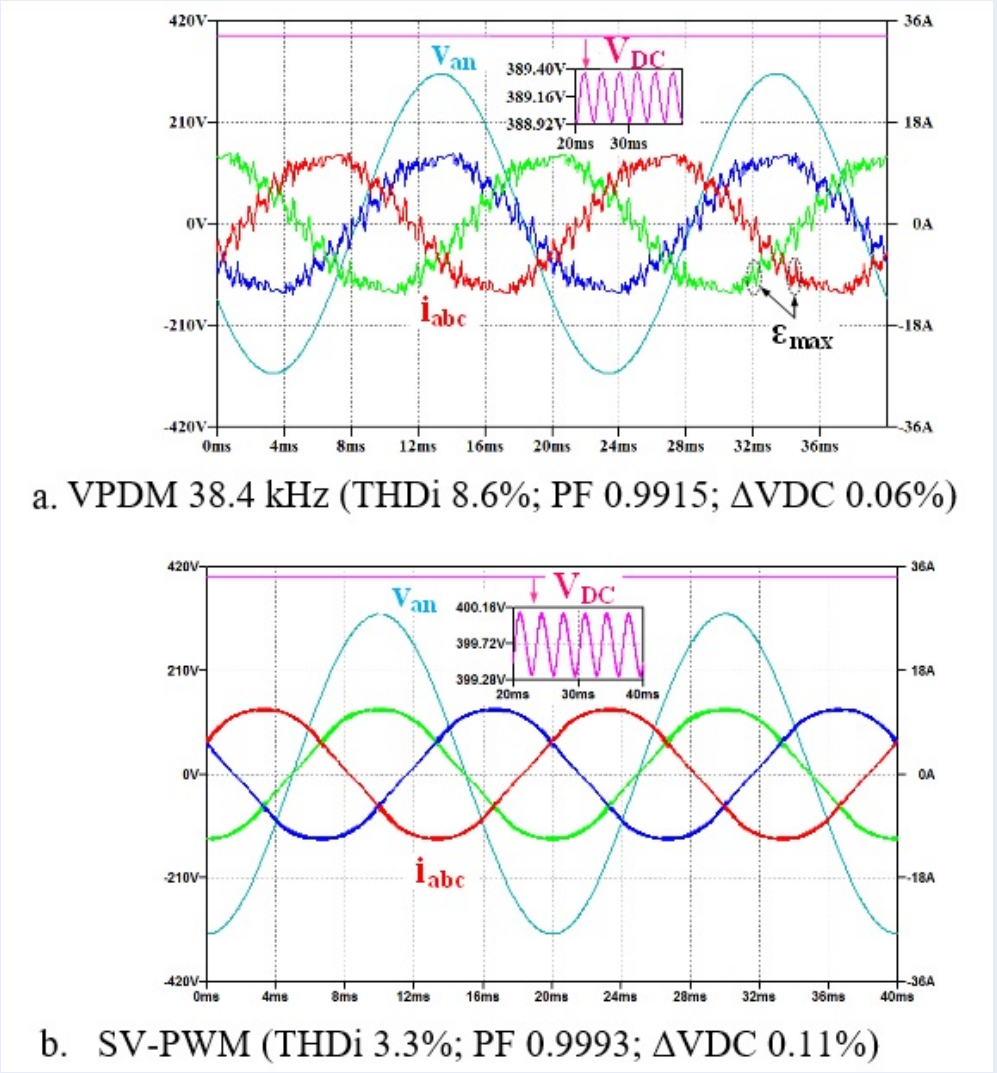


Figure 11: Simulation results

SYNCHRONIZATION METHOD FOR THE VPDM

In practice, a small variation in line frequency is allowed in all standards; hence, line frequency synchronization must be performed. For online algorithms, such as SV-PWM, this could be a challenge in power converters when the switching frequency passes 100 kHz. For the proposed offline VPDM, sampling is unnecessary; however, the line period is not necessarily an integer multiple of the PDM block, necessitating a line frequency synchronization algorithm for experiments.

Due to the symmetry in pulse density between two adjacent sectors, only one lookup table (LUT-1) is needed to store the pulse density value for each block. In FPGA, a counter Bb is used to maintain the block index for retrieving the pulse density value of the current block. After obtaining this pulse density, the corresponding PDM pattern can be determined with another lookup table (LUT-2f), in which another counter n_b is used to track the current switching cycle in the block. Let B_B be the maximum possible number of blocks, $\triangle f_g\%$ be the allowable frequency variation, and Bbs be the block index at which line frequency synchronization starts for that sector. The nominal line frequency and the switching frequency will set BB (an integer value), while B_{bs} should be an integer and chosen according to (20).

$$B_{bs} \leq B_B - \triangle f_g\%.\frac{f_s}{6B_B.f_{grid}}$$

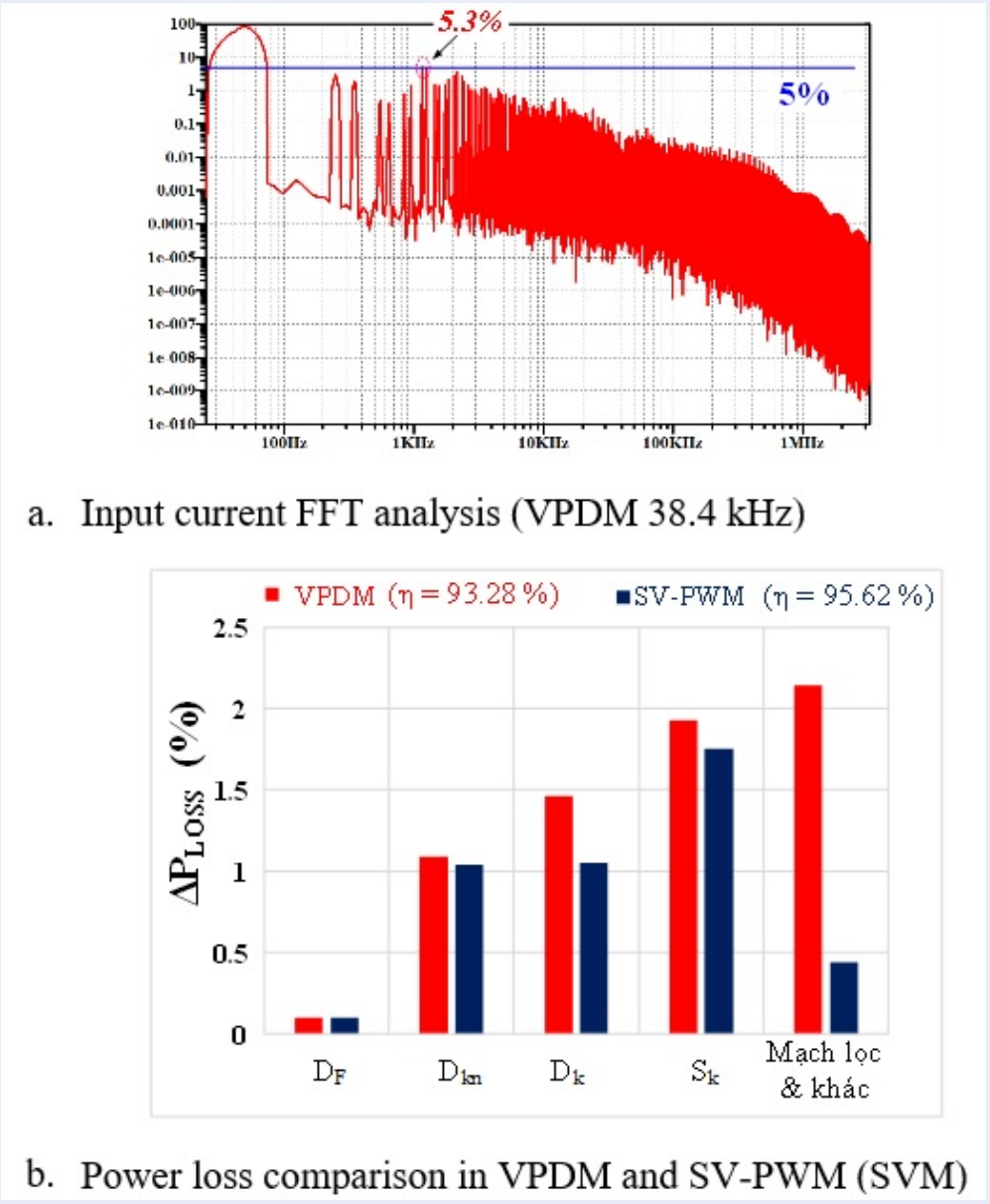


Figure 12: FFT analysis and power loss comparison (in simulation)

A flowchart of the proposed line frequency synchronization algorithm for an FPGA is shown in Figure 14. At the transition between an even sector and an odd sector, for example, from sector 12 to sector 1, the counter B_b starts at the lowest index and increases until it reaches the highest index BB in the LUT-1. When the counter value is equal to B_{bs}, the FPGA should start the line frequency synchronization algorithm to account for the highest allowable line frequency. If the line frequency is low enough, the counter should be able to reach the highest index B_B and stay there until the sector transition. After the sector transition, when the odd sector starts, the counter will decrease to the lowest value index in the LUT-1 and stay there until the next sector transition. This process is repeated at the transition between an even sector and an odd sector; hence, six times the input current waveform is synchronized with the input voltage waveform in any main period.

With the proposed line frequency synchronization method, for any main period shorter than the total time of all blocks in LUT-1, the FPGA can easily de-

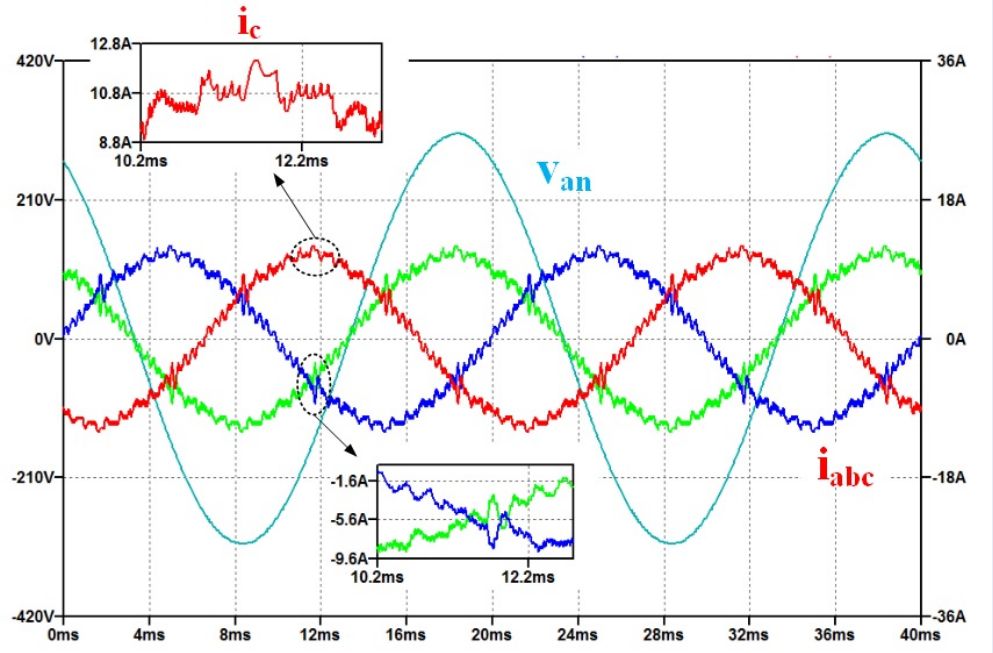


Figure 13: VPDM 174 kHz (THDi 4.3%; PF 0.9962)

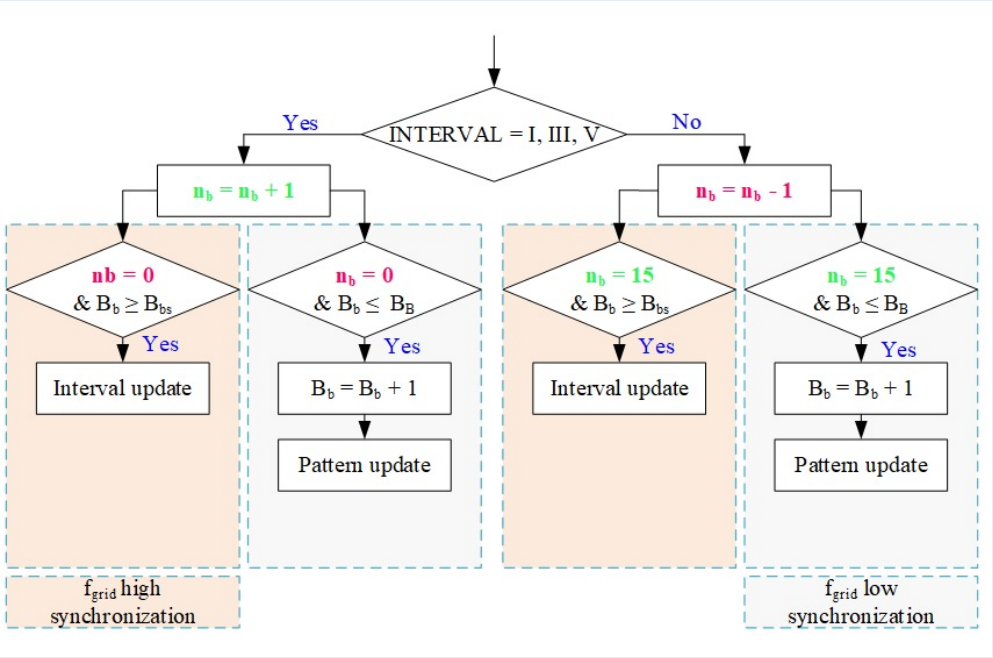


Figure 14: VPDM Synchronization method

tect sector transitions before reaching the highest index in LUT-1. For example, if the line frequency is 5% higher than the nominal frequency, which means that it is 52.5 Hz, then the transition should be approximately 7.6 blocks (for a 38.4 kHz switching frequency, and B_B is 8). On the other hand, if the line frequency is lower than the nominal value, the FPGA should reach the end of LUT-1 and wait for the sector transition. A large pulse density is maintained for the most active input phase so that at the peak of the current waveform, distortion can be limited, leading to low input current harmonic distortion. The experimental results in the next section prove the feasibility of the proposed modulation method and the proposed line frequency synchronization algorithm for 3SWCSR.

V. EXPERIMENTAL RESULTS AND DISCUSSION

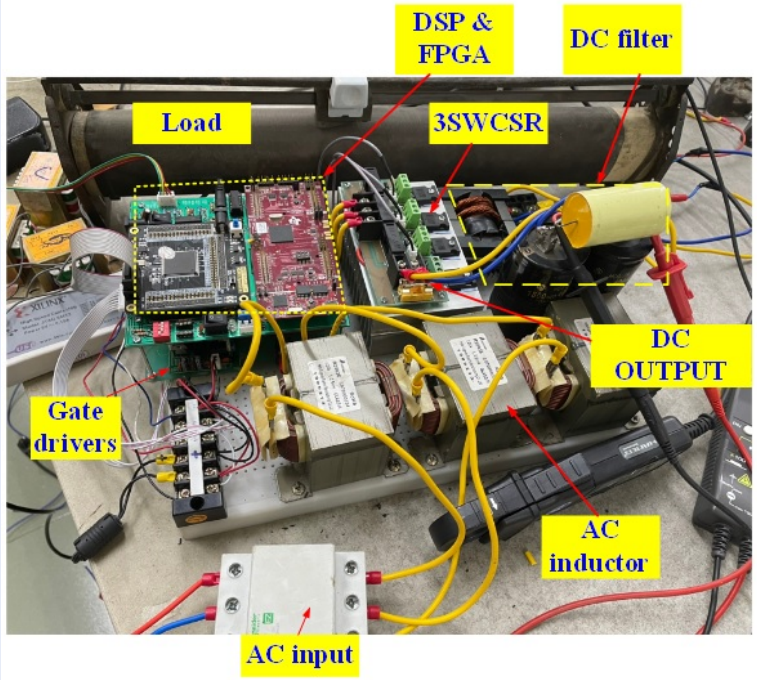
The simulation results in section III prove the feasibility of the offline VPDM, combined with the line frequency synchronization method proposed in section IV, applied to the 3SWCSR. To verify the practical performance of the converter, a 2 kW – 38.4 kHz prototype of the 3SWCSR, as shown in Figure 15a, with the basic parameters in Table 3, was implemented. A block diagram of the implemented VPDM on an FPGA (XC6SLX9-2TQG144C) and DSP F28379D is shown in Figure 15b, in which the inputs of the controller include a zero-crossing detector (ZCD) to detect the input sector and DC voltage sensor. The calculated values of pulse width D to obtain the demand DC voltage V_{DC}*, together with the input sector information, are transferred from the DSP to the FPGA, and the FPGA determines the needed PDM pattern from lookup tables and the gating signals to control isolated gate drivers. An input filter is needed to clean up the voltage signals before feeding to the ZCD to implement VPDM and line frequency synchronization. The experimental results are shown in Figure 16 and Figure 17.

In Figure 16, the phase A input current i_a waveform (red), phase A input voltage v_{an} waveform (blue), gating signals for S_a (D_0), S_b (D_1), and S_c (D_2), gating signal for S_a in the positive mains half-cycle (D_7), and negative mains half-cycle (D_6) are shown. Input voltage (red) and input current (blue) waveforms for phase A are shown in Figure 17a, and the output DC voltage V_{DC}, input currents i_a and i_c waveform, and input voltage v_{an} waveform are shown in Figure 17b. Waveforms were obtained by RIGOL DS-1102D (2 channels) and Gwinstek GDS-2064 (4 channels) DSOs. Harmonic distortion and the power factor were measured by a HIOKI CM3286-01 AC clamp power meter.

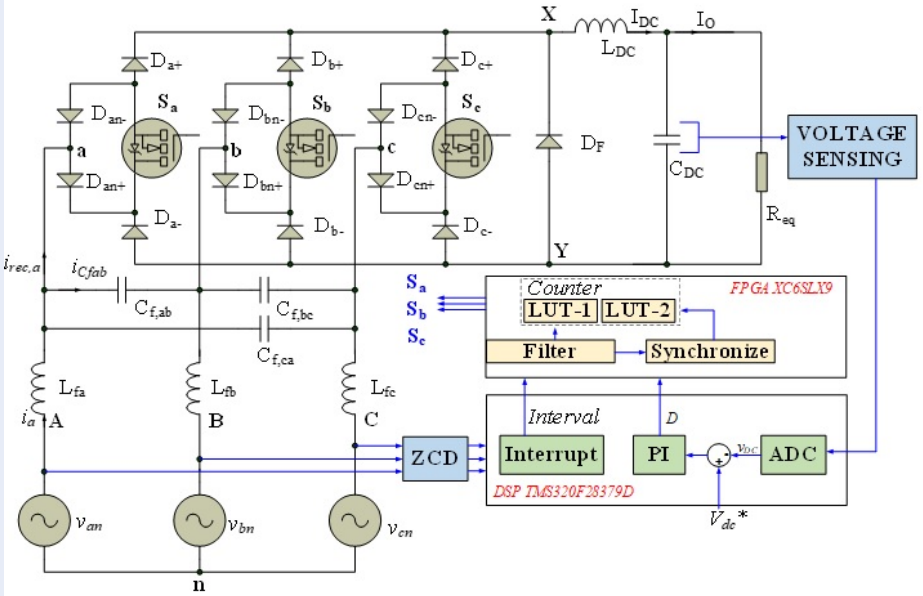
From the experimental results, the feasibility of the VPDM on the 3SWCSR has been shown for a low ripple (6.25%) DC output voltage, with a good input power factor (better than 0.9) and better input current THD (15.11%) than that of a diode rectifier (normally higher than 30%), or that of a basic SV-PWM algorithm (16.6%) [25]. The 3SWCSR has been tested at a 38.4 kHz switching frequency suitable for power switches under hard switching, with current glitches at sector boundaries leading to an input current THD higher than the limit suggested by the IEEE-519 standard [1], which is in good agreement with the simulation result of 8.6% presented in section III. The experimental results show a high power factor close to the results obtained in the simulation, proving that the synchronization process is well implemented to ensure phase synchronization between the current signal and the source voltage. However, the input current harmonics are more different in the experiment because the effects due to resonance between filters and parasitic components are ignored in the simulation. However, with these experimental results, the feasibility of the proposed algorithms has been proven, and it is possible to increase the switching frequency to achieve better input quality, depending on the power switches being used.

CONCLUSION

This paper proposed an offline variable pulse density modulation (VPDM) algorithm for a three-switch current source rectifier (3SWCSR) to achieve a high input power factor and reduced input current total harmonic distortion, with simple and effective implementation, especially when increasing the switching frequency. The algorithm can control the output voltage of the 3SWCSR over a wide range and needs to be implemented only by a PI controller, while the three-phase input sinusoidal waveform is achieved by means of offline FPGA-based lookup tables without any sampling operation. Therefore, it is advantageous to increase the switching frequency of the system. In addition, a synchronization algorithm with respect to the grid frequency is proposed to ensure the operation of the converter under changing grid conditions. The simulation and experimental results basically prove the feasibility of the proposed modulation, with a low-output DC voltage ripple of 6.25%, a high input power factor of 0.94, and an input current total harmonic distortion that is half of that in traditional uncontrolled rectifiers. In addition, simulation results also show that when the frequency is increased to 174 kHz, the input current harmonic quality is comparable to that of online algorithms.



a.Implemented experimental prototype



b. Block diagram of prototype control scheme

Figure 15: Experimental prototype

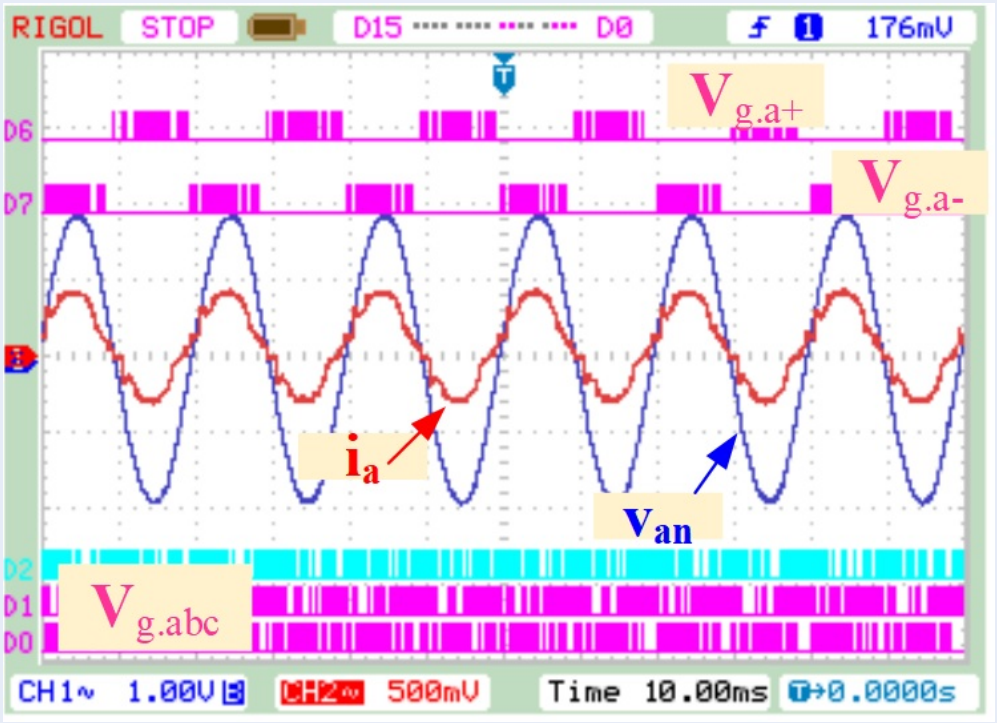


Figure 16: Gate driver signals in FPGA and input waveforms.

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LIST OF ABBREVIATIONS

CSRs: current source rectifiers
SHE/SHC-PWM: selective harmonic elimination/compensation pulse width modulation.
SV-PWM: space vector pulse width modulation
CB-PWM: carrieer-based pulse width modulation
DSP: digital signal processor
VPDM: Variable pulse density modulation
LUT: Look-up table
ZCD: Zero-crossing detector
ACRDCL: Active-voltage clamped resonant DC link

AUTHORS' CONSTRIBUTION

Thuong Ngo-Phi proposed the research idea and conducted simulations and experiments.
Nguyen Dinh Tuyen contributed to the technical background and proof reading.
Nam Nguyen-Quang contributed to the technical background, hardware implementation, and proof reading.

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CONFLICT OF INTEREST

The authors confirm that they do not have any conflict of interest in completing this paper.

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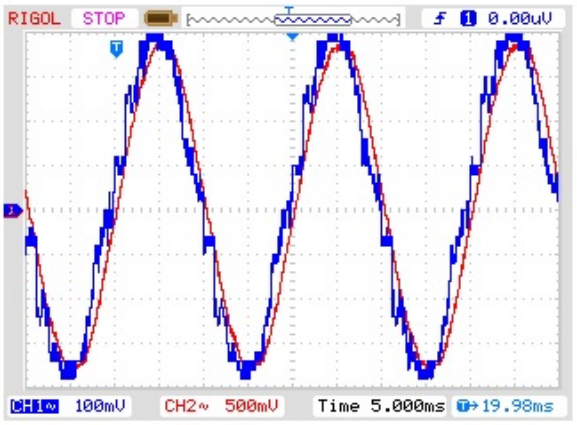
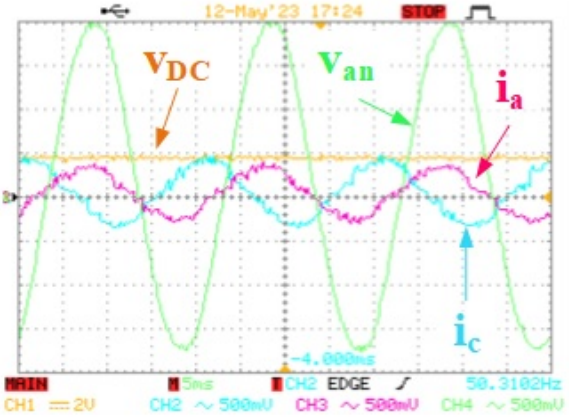


a. Input voltage V_{an} (red, ≈ 100 V/div) and current i_a (blue, 1 A/div) (**15.11%** THDi; **0.943** PF)



b. Input and output waveforms (V_{DC}, orange, 200 V/div, ΔV_{DC} **6.25%**)

Figure 17: Experimental waveform results

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