DSP-based pulse width modulation generator for very Spare Matrix Converter

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(Manuscript Received on July 15, 2015, Manuscript Revised August 30, 2015)

ABSTRACT

This paper present a modulation scheme for the Spare Matrix Converter (SMC) topology. The proposed method uses the space vector modulation (SVPWM) technique to control the converter's rectifier stage and inverter stage. This method achieved the maximum modulation ratio of 0.866 with sinusoidal input/output current waveforms.

In the other hand, a simple real-time implementation method avoiding additional CPLD or FPGA devices is introduced. This technique is verified through simulation results using PSIM software and experimental results a 32-bit floating-point DSP (TMS 320F28335).

Key words *- spare matrix converter, input filter, input power factor, matrix converter, space vector modulation.*

1. INTRODUCTION

The Matrix Converters are ac-ac power conversion devices that can provide flexible and controllable increment/decrement of both voltage and frequency amplitude. They have experienced a resurgence of attention recently [1]-[5] because of its advantages of adjustable power factor, bi-directional power flow, high quality input/output current waveform, and the possibility of a compact design due to the lack of large energy storage components. The absence of large energy storage elements in the dc bus such as the bulky and limited lifetime electrolytic capacitor is their major advantage over traditional ac/dc/ac topologies that allows size and weight reduction of the converter and increasing its reliability as well.

The development of MCs began in the early 1980's when Alensia and Venturini introduced the basic principles of operation [6]. Afterwards, the MCs are applied to adjustable motor speed drive, renewable energy, distributed power generation systems and many others [7]-[9].

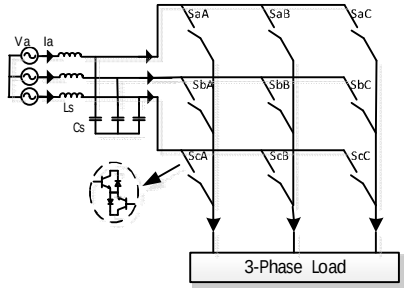

Figure 1. The direct matrix converter topology.

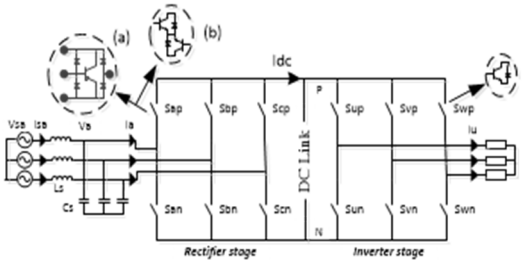

Figure 2. (a) The spare matrix converter topology (b) the indirect matrix converter.

The MCs is divided into two categories: direct matrix converter (DMC) and indirect matrix converter (IMC) [10], [11]. The DMC includes nine bidirectional switches [12-13], as show in Figure 1. The main circuit of the IMC has two stages: rectifier has six bidirectional switches and inverter has six directional switches, as show in Figure 2 (b) [14]. Both of two converters are able to generate input/output waveforms with the same performance and the same voltage transfer ratio capability. The LC input filter consists of three inductors and three capacitors, acts as an interface between the power supply and converter. They need to reduce the current harmonics injected into the main. This paper focuses on analyzing the SMC topology because it has several advantages such as easy implementation, more secure commutation technique, the possibility of further reducing the number of power switches and the possibility of modifying.

On the other hand, the digital implementation of the switching patterns for the SMC is a hard task to the high complexity of matrix convert's modulation schemes. The last few years, the authors proposed several modulation algorithms to solve this problem. In [15] and [16], proposed the use of DSP boards that can be connected directly into the PCI bus of a desktop computer, this method is not suitable for industrial applications because of bulk and expensiveness.

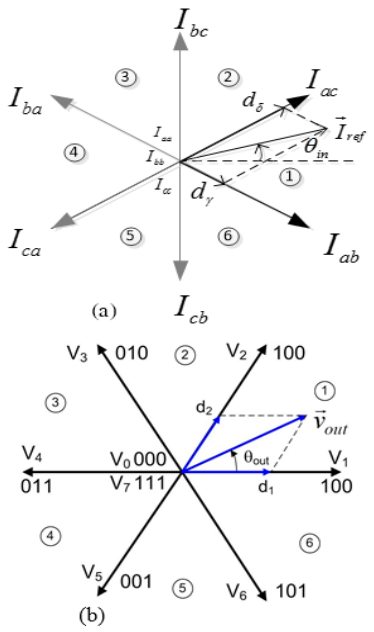

Figure 3. (a) The diagram space vector of the rectifier stage (b) The diagram space vector of the inverter stage.

Other proposals use a microcontroller combine with logic circuits. The methods above-mentioned, the obtained switching frequency is not high enough so as to increase the power density of the converter as suggested by today's technology. Recent years, the use of a DSP combine with a FPGA module has been applied in many power electronics. In this core, the communication between the two chips: DSP and FPGA. The fist, DSP calculates duty cycles at every sampling period of the input current and output voltage. The results are transmitted to FPGA chip through a data transfer bus. The second, an interface block should generate the opportune gating pulse for the converter's IGBT. However, data transmission between the DSP and the FPGA is essential to synchronize the timing of the different events in the two chips. The other paper proposed a DSP-FPGA-base implementation method wherein no data transfer

or synchronization signals between the DSP and the FPGA.

This paper uses the SVPWM technique to control the rectifier stage and inverter stage. On the other hand, a simple real-time implementation method that avoids the use of logical circuitry such as CPLD/FPGA devices was also presented.

This paper is organized as follows: A review of the SMC topology operation and the conventional SVM principle are presented in the next section. Describes a real-time implementation method in section 3. The simulation and experimental results are provided in section 4 and 5, respectively. Some conclusions are given in the last section.

2. OPERATIONAL PRINCIPLES OF SMC AND CONVENTIONAL SVM METHOD

2.1 Operational Principles of SMC

The power circuit of the SMC feeding three-phase inductive load is shown in Figure 2(a). It consists of a current source rectifier connected to a voltage source inverter. A input filter is added between the mains and the rectifier to reduce the current harmonics injected into the power supply. The voltages and currents at the ac source side are denoted by $V_{sa,b,c}$ and $i_{sa,b,c}$ respectively. $i_{a,b,c}$ are the switched currents at the input side of the converter. The phase-to-neutral output voltage and output current are denoted by $V_{u,v,w}$ and $i_{u,v,w}$. The current flowing through the dc bus connecting the two stages is denoted by i_{dc}. Six bidirectional switches of rectifier stage which are $S_{ap,bp,cp,an,bn,cn}$, is directly connected six unidirectional switches $S_{up,vp,wp,un,vn,wn}$ of the inverter stage.

The rectifier stage is controlled in such a way to provide sinusoidal input currents with unity input power factor. It is maintain the maximum positive voltage in the dc-link as well as maintain the sinusoidal waveform in input currents. The inverter stage controls the voltage out with variable frequency and amplitude. The basic control strategy for SMC is based on the space vector analysis of input current and output voltage.

2.2 Conventional SVM Method

In the conventional SVM approach for SMC, the operation of the rectifier stage depends only on the phase angle and instantaneous value of the input voltage. It is aassumed that the SMC is connected to a balanced three-phase power supply, which is given as follows:

$$\begin{aligned} v_{sa} &= V_{in}\cos\left(\omega_{in}t+\varphi_{in}\right) \\ v_{sb} &= V_{in}\cos\left(\omega_{in}t+\varphi_{in}-2\pi/3\right) \\ v_{sc} &= V_{in}\cos\left(\omega_{in}t+\varphi_{in}-4\pi/3\right) \end{aligned} \quad (1)$$

The three-phase desired output voltages are described by

$$\begin{aligned} v_{u} &= V_{out}\cos\left(\omega_{out}t+\varphi_{out}\right) \\ v_{v} &= V_{out}\cos\left(\omega_{out}t+\varphi_{out}-2\pi/3\right) \\ v_{w} &= V_{out}\cos\left(\omega_{out}t+\varphi_{out}-4\pi/3\right) \end{aligned} \quad (2)$$

where, V_1 and V_2 are the magnitude of input and output phase voltages.

ω_{in}, ω_{out} is the input and output angular frequency.

φ_{in}, φ_{out} is the initial phase angle of input and output phase voltage.

The space vector diagram of the rectifier stage and the inverter stage includes six active vectorsand three zero vectors as shown in Figure 3.

To explain the modulation technique of SMC, it is assumed that both the reference input current and the reference output voltage vector to be located in sector 1 ($-\pi/6 \le \theta_{in} \le \pi/6$ and $0 \le \theta_{out} \le \pi/3$), where θ_{in} and θ_{out} are the angles within their respective sectors of the input current and the output voltage reference vectors.

2.2.1 Rectifier stage

The space vector of the rectifier stage is composed of six active current vectors with fixed directions and three zero vector, as shown in Figure 3(a). The reference current vector is generated from to active current vector.

In sector 1, the reference input current vector I_{ref} can be synthesized by using two active vector I_{ab} and I_{ac}. The switch S_{ap} is always on while S_{bn} and S_{cn} are modulated. The duty cycle of two switches S_{bn} and S_{cn} are given as:

$$d_\gamma = m_i \sin(\pi/6 - \theta_{in}) \quad (3)$$

$$d_\delta = m_i \sin(\pi/6 + \theta_{in}) \quad (4)$$

where m_i is the rectifier stage modulation index.

In the rectifier stage, the zero vectors are not considered. Hence, the switching sequence only consists of the two active current vectors I_{ab} and I_{ac}, whose duty cycles are given by

$$d_x = d_{ab} = \frac{d_\gamma}{d_\delta + d_\gamma} = -\frac{v_b}{v_a} \quad (5)$$

$$d_y = d_{ac} = \frac{d_\delta}{d_\delta + d_\gamma} = -\frac{v_c}{v_a} \quad (6)$$

During one sampling period, the dc-link voltage is modulated with two line-to-line input voltages. While S_{bn} is turned on, the dc-link voltage equals to v_{ab}, and while S_{cn} is turned on, the dc-link voltage equals to v_{ac}.

The average dc-link voltage is obtained as follows:

$$V_{dc} = d_{ab}(v_a - v_b) + d_{ac}(v_a - v_c) = \frac{3}{2}\frac{V_{in}^2}{v_a} \quad (7)$$

From (4), the minimum value of the average dc-link voltage is $V_{dc(\min)} = \frac{3V_{in}}{2}$ (8)

We can find the switching states, the corresponding dc-link voltage and its average value for any other input sector by utilizing the same approach, and the results are summarized in Table I.

2.2.2 Inverter stage

Once the switching state of the rectifier stage is determined, the traditional SVPWM can be applied to control the inverter stage. For calculating the duty cycles of the active and zero vectors in the inverter stage, it is necessary to refer to the local average dc-link voltage value. The eight space vectors with the six active vectors (V_1~V_6) and the two zero vectors (V_0, V_7) are used in the SVPWM method.

For a reference output voltage vector with the magnitude, V_{out}, and phase angle, θ_{out}, in sector 1 shown in Fig. 3(b), the duty cycles of two active vectors V_1, V_2 and two zero vectors V_0, V_7 are given as follows:

$$\begin{aligned} d_1 &= \sqrt{3}\frac{V_{out}}{V_{dc}}\sin(\pi/3 - \theta_{out}) \\ d_2 &= \sqrt{3}\frac{V_{out}}{V_{dc}}\sin(\theta_{out}) \\ d_0 &= d_7 = 0.5(1 - d_1 - d_2) \end{aligned} \quad (9)$$

where d_0, d_1, d_2 and d_7 are duty cycles of V_0, V_1, V_2 and V_7, respectively.

And, the voltage transfer ratio of the SMC, m, is defined as follows: $m = \frac{V_{out}}{V_{in}}$ (10)

According to (4) - (7), the voltage transfer ratio should be smaller than 0.866 in order to maintain all duty cycles positive.

To obtain the balanced input current and output voltage, the switching patterns for the rectifier and the inverter stage should be combined effectively.

Table 1. The Switching States and Dc-link voltage according to the Input Sector

Input sector	Conducting switch	Modulated switches	Dc-link voltage	Average value (V_{dc})
1	S_{ap}	S_{bn}, S_{cn}	v_{ab}, v_{ac}	$3V_{in}^2/2v_a$
2	S_{cn}	S_{ap}, S_{bp}	v_{ac}, v_{bc}	$-3V_{in}^2/2v_c$
3	S_{bp}	S_{an}, S_{cn}	v_{ba}, v_{bc}	$3V_{in}^2/2v_b$
4	S_{an}	S_{bp}, S_{cp}	v_{ba}, v_{ca}	$-3V_{in}^2/2v_a$
5	S_{cp}	S_{bn}, S_{an}	v_{cb}, v_{ca}	$3V_{in}^2/2v_c$
6	S_{bn}	S_{ap}, S_{cp}	v_{ab}, v_{cb}	$-3V_{in}^2/2v_b$

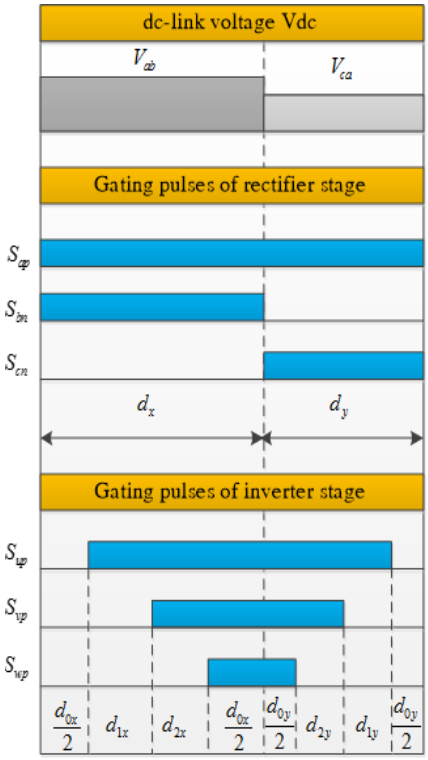

Figure 4. Transistors' gating pulses when the input current and output voltage reference vectors are assumed to be both lying within sector 1.

As mentioned before, the dc-link voltage has two values v_{ab} and v_{ac} during one sampling period with the duty cycles d_{ab} and d_{ac}, respectively. Therefore, the switching states at the inverter stage are divided into two groups as shown in Figure 4. The duty cycles of two active and two zero vectors in each group are calculated as follows:

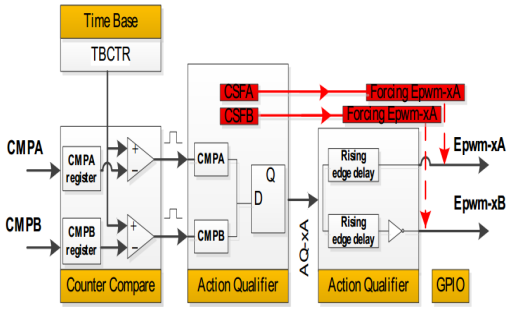

Figure 5. Simplified block diagram of an epwm module

$$d_{1x} = d_1 d_x ; d_{2x} = d_2 d_x ; d_{0x} = d_{7x} = d_7 d_x \quad (11)$$

$$d_{1y} = d_1 d_y ; d_{2y} = d_2 d_y ; d_{0y} = d_{7y} = d_7 d_y \quad (12)$$

3. DESCRIBES A REAL-TIME IMPLEMENTATION METHOD

In recent literature, the gating pulses of Spare Matrix Converter switches used the DSP-FPGA. The use of a FPGA in conjunction with external processors such as DSPs or rapid prototyping controllers (dSPACE) remains up to now a competitive solution in most power electronic and motion control applications [22]-[26]. However, the real-time implementation of the IMC topology must use two chips which make cumbersome. To reduce the complexity of the SMC: 1. the use of a single FPGA chip with an embedded processor would be a more compact solution. However, this will make much more difficult the implementation of intensive arithmetic operations and trigonometric calculation. 2. The use only the DSP.

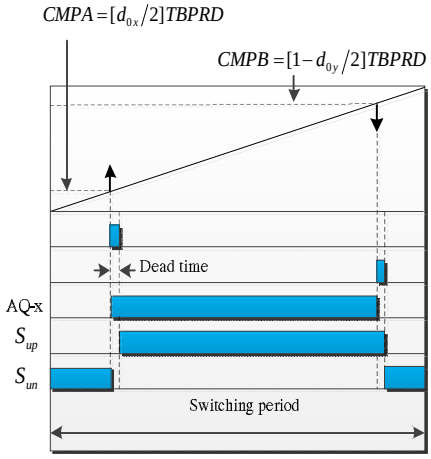

Figure 6. Synthesize of gating pulses of S_{up} and S_{un} inverter stage.

In this paper, a straightforward implementation method that uses only the epwm modules of the DSP TMS320F28335 is presented. A simplified block diagram of an epwm modules of which can generate two independent 16-bit pwm signals (epwm-xA and epwm-xB) on the GPIO peripheral of the DSP in Figure 5. The attractive feature of these modules is that for a fixed switching

frequency operation, two compare registers have to be reloaded by the CPU at each sampling period, able to generate higher switching frequency higher pulse resolution pwm signals with a minimum CPU overhead. Moreover, by an suitable configuration of the two couples of bits CSFA and CSFB, they are able to impose high/low levels on the outputs epwm-xA and epwm-xB. CSFA and CSFB receive three values (00/ 01/ 11) which correspond to the following actions on outputs epwm-xA and epwm-xB:

- CSFA: (00) forcing disabled, (01) forces a continuous low on output A, (10)
- forces a continuous high on output A.
- continuous high on output A, (10) **forces a continuous low on output A.**

3.1 Inverter stage control:

The gating pulses for the output stage three upper and three lower IGBT will be generated by epwm1A, epwm2A, epwm3A and epwm1B, epwm2B, epwm3B. To clarify the approach, we consider the gating pulse of S_{up} as illustrated in Figure 4. The pulse of S_{un} is obtained simply by inverting the one of S_{up}. This case, the output voltage reference vector varying within sector 1, the opportune values loaded within the two compare registers are $CMPA = [d_{0x}/2]TBPRD$ and $CMPB = [1-d_{0y}/2]TBPRD$. *TBPRD* is the maximum counting value of the time base counter *(TBCTR)* that is treated as the input while the generated event *TBCTR = CMPA* or *TBCTR = CMPB* is expect output. When *TBCTR = CMPA*, epwm1A will be set active high; while *TBCTR = CMPB*, epwm1A will be set active low and *TBCTR* is incrementing as shown in Figure 6. For practical safety consideration, a dead band should be inserted into the ideal PWM waveform to avoid that the two IGBTs on the same bridge led of the inverter. Therefore, the dead band submodule generates the two complementary pwm signals with programmable turn-on delay times.

3.2 Rectifier stage control

Just to simplify, we considered the reference input current vector to be located in sector 1, the gating pulse of power switches depicted in Figure 4. In this sector, the gating pulse of S_{bn} and S_{cn} is modulated while the one of S_{ap} is force to a high level and the one of S_{an}, S_{bp}, S_{cp} is force to a low level. Assume that the output signals epwm-xA and epwm-xB feed the gates of S_{ap}, S_{bp}, S_{cp} and the gates of S_{an}, S_{bn} , S_{cn} respectively (x = 4, 5, 6). In this situation, the opportune values assigned to the epwm module compare register are summarized in Table II. The signal AQ-X generated by the Action Qualifier sub module (AQ) is high when the time base counter equals CMPA value and set to a low stage when the time base counter equals CMPB value as illustrated in Figure 7.

The signal epwm-xB feeding the gates of IGBT S_{an}, S_{bn}, S_{cn} is constructed from AQ-X that passes through the falling edge delay block and the inverting gate of the Dead Band submodule. Thereafter, the output epwm-xB generates a pulse with a tune-on delay time as depicted in Figure 7.

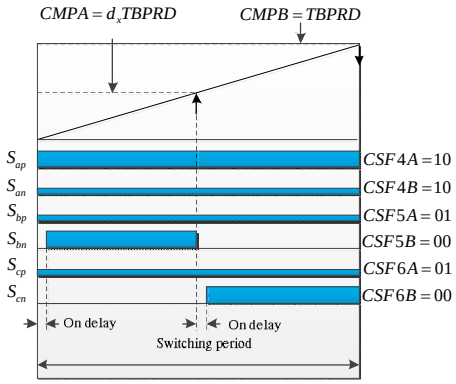

Figure 7. Synthesize of gating pulses of switches of rectifier stage in sector 1.

4. EXPERIMENTAL RESULTS

In order to validate the effectiveness of the implementation method, an Indirect Matrix Converter prototype was setup experimentally. A

simplified block diagram of the converter and the controller board is shown in Figure 8.

The converter is feeding a three phase star connected R-L load (R = 10Ω and L = 25mH) and supplied to grid though an LC filter (L = 1mH, and C = 25μ). The main control algorithm implemented by a 32-bit DSP (TMS320F2812 by Texas Instruments) operating with a clock of 150MHz, consists of the fundamental blocks which determines the position of the input current reference vector in the complex plane, computes the instantaneous phase angle of grid voltage, computes the duty ratios and determines the opportune values of CMPA and CMPB registers of each epwm module.

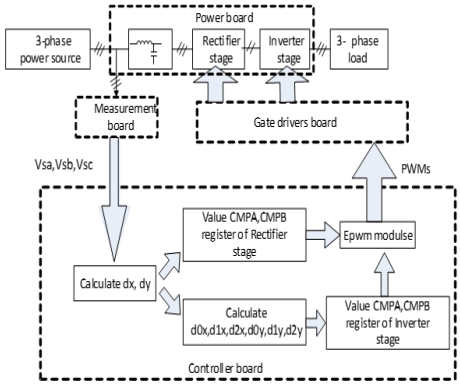

Figure 8. Simplified block diagram of the converter and control algorithm.

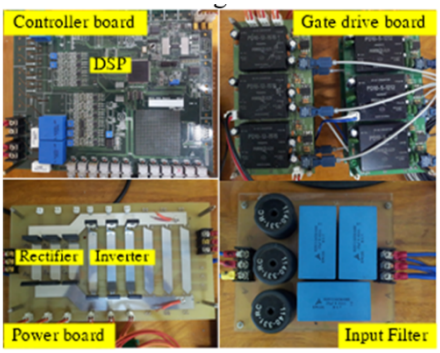

Figure 9. The photograph of the experimental setup.

The photograph of the experiment equipment is shown in Figure 9. The power circuit of the rectifier stage is constructed by six discrete IGBTs (FIO 50-12BD) and the inverter stage is composed of three dual-IGBTs (FGH60N60SMD).

The PWM period of the system is set with 100 μs. All experimental parameters are same as those in the simulation.

Figure 10 shows the experimental PWM signals for six bidirectional switches in the rectifier stage. It can be observed that, in each time, only two switch remains high state and in each sector, one switch is always high state and two switches are modulated. For example, in sector 1, the switch S_{ap} is high state and two switches S_{bn} and S_{cn} are modulated.

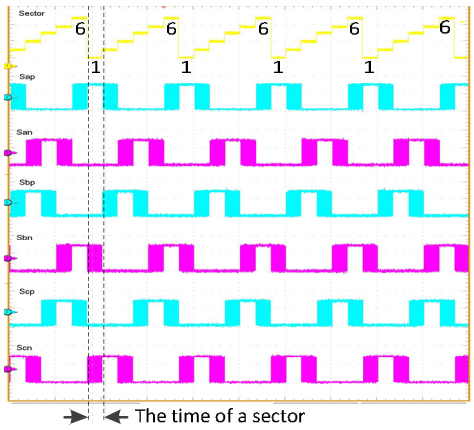

Figure 10 The experimental PWM signals for six bidirectional switches of rectifier stage.

The experimental results shown in Figure 11 is the dc-link voltages which is generated by rectifier stage. The dc-link voltage waveforms are not affected by the inverter stage control and do not decrease to zero because no zero switching states in the rectifier stage are used. It is modulated between two line-to-line voltages.

Figure 12 display a modulate line-to-line output voltages and the load current waveforms obtained with a voltage transfer ratio q=0.75 and output frequency fo=50Hz. It can be seen that, the peak line-to-line output voltage is the same as line-to-line input voltage and the load current is quite sinusoidal.

The input current of SMC before filter (i_a), input current of power supply after filter (i_{sa}) and phase voltage (V_{sa}) are shown in Fig. 13 and Figure 14.

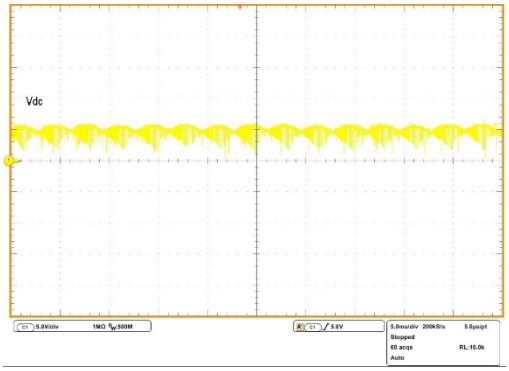

Figure 11. The experimental results of dc-link voltage.

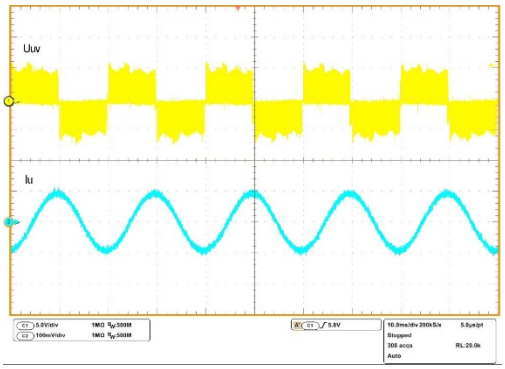

Figure 12. The experimental results of output phase voltage and output phase current.

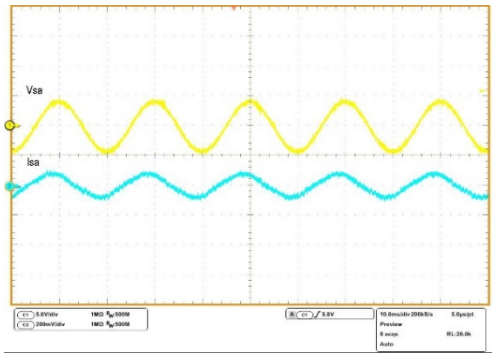

Figure 13. The experimental results of input phase voltage and input current after filter.

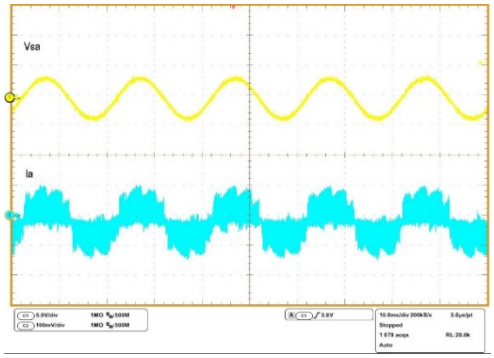

Figure 14. The experimental results of input phase voltage and input current before filter.

As can be seen, input current of SMC is in phase with the input voltage and sinusoidal, balanced, and free of low-order harmonic components. However, the input filter causes the phase angle difference between the voltage and current of the power supply and the displacement angle between the source line current i_{sa} and the rectifier input current i_a.

5. CONCLUSIONS

A new real-time implementation method of SVM algorithm for the Spare Matrix Converter is presented, evaluated. This method uses the SVPWM approach to control the rectifier stage and the inverter stage. A simple real-time implementation method without the use of CPLD or FPGA was presented leading to the only use of DSP controller which further simplifies the control platform. The new method allows a compact design, low-cost, and easier implementation. The performance of the proposed SVM is verified by both simulation and experiment.

ACKNOWLEDGEMENT

This research is funded by Vietnam National University Ho Chi Minh City (VNU-HCM) under grant number C2014-20-23

Kỹ thuật tạo xung PWM cho biến tần ma trận dựa trên DSP

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TÓM TẮT

Bài báo trình phương pháp xuất xung cho biến tần Spare Matrix Converter. Phương pháp được đề xuất sử dụng kỹ thuật điều chế vector không gian để điều khiển tầng chỉnh lưu và tầng nghịch lưu của bộ biến đổi. Phương pháp này đạt tỉ số điều chế lớn nhất là 0.866 với dạng sóng của dòng điện ngõ vào/ra sin. Phương pháp thực hiện thời gian thực đơn giản tránh việc thêm vào những thiết bị như CPLD hoặc FPGA được giới thiệu trong bài báo này. Kỹ thuật này được kiểm chứng thông qua kết quả mô phỏng sử dụng phần mềm PSIM và kết quả thực nghiệm sử dụng 32-bit DSP (TMS 320F28335).

Từ khóa: *biến tần spare matrix converter, bộ lọc ngõ vào, hệ số công suất ngõ vào, matrix converter, điều chế vector không gian.*

REFERENCES

[1] M. Venturini and A. Alesina, "The generalized transformer: A new bidirectional sinusoidal wave form frequency converter with continuously adjustable input power factor '' in Proc. IEEE PESC'80, vol.1, pp.237-247.

[2] P. Nielsen, F. Blaabjerg and J. Pedersen, "New protection issues of a matrix converter: design considerations for adjustable-speed drives" IEEE Trans. On Industry Applications, vol. 35, No.5, 1999, pp. 1150-1161.

[3] M. Marcks, "A new double resonant zero current switching matrix converter", In proceedings of EPE'1995 conference, pp.2.100-2.105.

[4] Burany, N, "Safe control of four quadrant switches", In Proceedings of IAS 1989, pp. 1190- 1194.

[5] J. Mahlein, J. Igney, J. Weigold, M. Braun, and O. Simon, Matrix Conveter commutation strategies with and without explicit input voltage sign measurement", IEEE trans. On Industrial Electronics, vol. 49, No.2, 2002, pp. 407-414.

[6] Alesina and M.G.B. Venturini "Solid-state power conversion: A Fourier analysis approach to generalized transformer synthesis," IEEE Trans. Circuits and Syst., Vol.28, No.4, pp. 319- 330, Apr. 1981.

[7] Kyo-Beum Lee and F. Blaabjerg, "Sensorless DTC-SVM for Induction Motor Driven by a Matrix Converter Using a Parameter Estimation Strategy," IEEE Trans. Ind. Electro. , vol.55, no.2, pp.512-521, Feb. 2008.

[8] S.L. Arevalo, P. Zanchetta and P.W. Wheeler, "Control of a Matrix Converter-

based AC Power Supply for Aircrafts under Unbalanced Conditions," in Proc. IECON 2007 pp.1823-1828.

[9] V. Kumar, R. R. Joshi and R.C. Bansal,"Optimal Control of Matrix-Converter-Based WECS for Performance Enhancement and Efficiency Optimization," IEEE Trans. Energy. Conver. vol.24, no.1, pp.264-273, March 2009.

[10] P. Correa, J. Rodriguez, M. Rivera, J.R. Espinoza and J.W. Kolar, "Predictive Control of an Indirect Matrix Converter," IEEE Trans. Ind. Electro., vol.56, no.6, pp.1847-1853, June 2009.

[11] M. Jussila, M. Eskola and H. Tuusa, "Analysis of non-idealities in direct and indirect matrix converters," in Proc. EPE - ECCE Europe 2005, pp.1 - pp.10, 2005.[6]

[12] P.W. Wheeler, J. Rodriguez, J.C. Clare, L. Empringham amd A. Weinstein, "Matrix Converters: a technology review,"IEEE Transaction on Industrial Electrics, vol.49, No.2, pp.276-288, Apr 2002.

[13] T.F Podlesak, D.C. Katsis, P.W. Wheeler, J.C. Clare, L. Empringham and M. Bland, "A 150kVA vector-controlled matrix converter induction motor drive,", IEEE Transation On Industry Applications, vol.42, No.3, pp.481-847, May-June 2005.

[14] Klumpner and F. Blaabjerg, "Two stage direct power converters: an alternative to the matrix converter," in Proceeding of IEE Seminar on Matrix Converters, April 2003, pp. 7/1- 7/9, [Digest No. 2003/10100].

[15] M. Hamouda, F. Fnaiech, and K. Al-Haddad, "A DSP based real-time simulation of Dual-Bridge matrix converters," in Proc. IEEE ISIE Conf.,Vigo, Spain, 2007, pp. 594–599.

[16] S. Müller, U. Ammann, and S. Rees, "New time-discrete modulationscheme for matrix converters," IEEE Trans. Ind. Electron., vol. 52, no. 6,pp. 1607–1615, Dec. 2005.