# A Design of 10-b 100-MS/s Pipelined Folding ADC with Distributed Track-and-Hold Preprocessing

- **Binh Son Le**
- **Trong Tu Bui**
  University of Science, VNU-HCM
- **Duc Hung Le**
  University of Electro - Communications, Tokyo, Japan

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## ABSTRACT

*This paper presents a 10-b ADC designed in a 0.18-μm CMOS technology. The ADC achieves 10-b resolution by using the cascaded folding technique in both the fine and coarse converters. Folding stages are pipelined to improve the settling time. As a result, this ADC can achieve the sampling rate up to 100MS/s. Moreover, instead of using a costly single track-and-hold circuit, a distributed track-and-hold circuit is used to reduce the chip area and the power consumption. This also allows utilizing the open-loop architecture of the folding technique, thus improving the performance of the system. The simulation results show that with a 49 MHz sine-wave input, the ADC consumes 66 mW and the effective number of bit (ENOB) is 9.28-b. Taking into account of process variations by using a Monte Carlo simulation, the DNL varies from ±0.45LSB to ±0.25LSB. The layout of the ADC occupies 1.2 mm$^2$ die area.*

***Keywords:*** *CMOS, ADC, High Speed, Folding*

## INTRODUCTION

Over the past decades, the development of CMOS technology has led to a dramatic growth of high performance digital signal processing systems. And since analog-to-digital converters (ADCs) play as the bridge between the analog and digital world, the speed and resolution requirements of ADCs have been pushed one-step further to achieve higher system performance. Because of its parallel architecture, flash ADC can be the fastest type of ADCs [1-3]. However, the cost of hardware complexity and power dissipation have limited their resolution below 10-b. On the other hand, two-step and pipelined ADCs use the information received after quantizing coarse bits to quantize fine bits.

Thus, these ADCs achieve higher resolution, but much slower than flash ADC. To sum up, the open-loop architecture of flash ADC is attractive for high speed, while the multi-step architecture of two-step and pipelined ADCs are necessary to improve resolution. Hence, for utilizing advantages of those architectures, folding ADC has been proposed by Rudy J. van de Plassche [4]. Since then, many new folding architectures have been proposed to improve speed and resolution while achieving lower hardware complexity and power dissipation.

In this paper, after reviewing techniques have been proposed over recent years, a 10-b 100-MS/s folding ADC will be designed based on

those architectures. The designed ADC allows a maximum input signal frequency up to the Nyquist frequency and dissipates 66 mW at 100 MHz sampling rate. In this study, the interpolating technique will be used to reduce the number of folding circuits, thus reducing the area and power consumption of the ADC. In order to achieve 10-b resolution, the cascaded folding technique [1, 5-8] is implemented. This technique is also combined with pipelining technique [5] to improve the performance of the ADC. Distributed track-and-hold (T/H) pre-amplifier [3, 4, 9] and averaging technique [1, 6, 10] have also been integrated into the design to improve dynamic performance and the DNL, respectively.

**PIPELINED CASCADED FOLDING ADC**

**Folding**

As depicted in Fig. 1, folding ADC simultaneously carry out coarse bits and fine bits quantization processes to maintain high conversion speed. Two types of folding circuits usually used are the cross-coupled differential pairs (CCDP) [2-7] and the Gilbert cell [11, 12], which are depicted in Fig. 2.
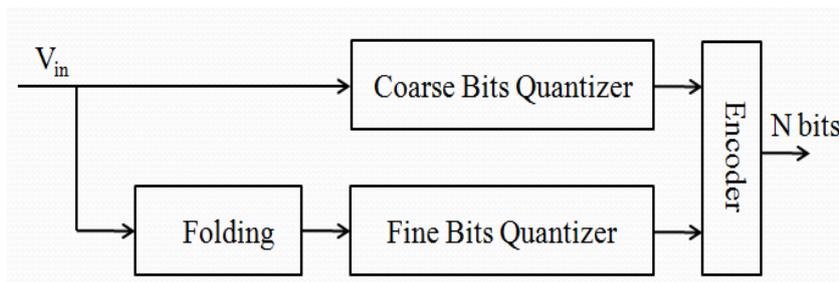


**Fig. 1.** Block diagram of a standard folding ADC

CCDP circuits can only be used with odd folding factor, have higher power dissipation, higher output capacitance and mismatches in current sources also affect zero-crossing points locations. But Gilbert cell has smaller linear dynamic range than CCDP circuits. Fig. 3 depicts an output signal of a CCDP circuit, it can be seen that the peaks of the output signal become rounded because of the changing between working regions of MOSFET. This non-linear effect poses some serious problems when designing a folding ADC.

Therefore, instead of using only one folding circuit to create one folding signal, many folding circuits will be used to generate $2^{Nfine\,bit}$ folding signals. Hence, distance between adjacent zero-crossing points will be 1 LSB as shown in Fig. 4. Although this method solves the linearity requirement of folding signals, it also leads to high power consumption and occupies large chip area. That is why the interpolating technique is integrated into folding ADC.
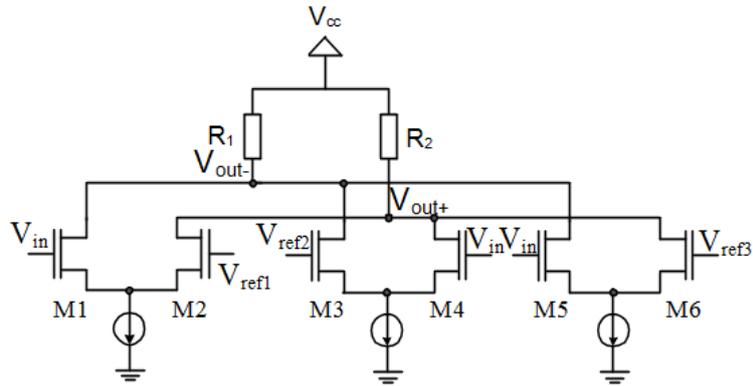
a)
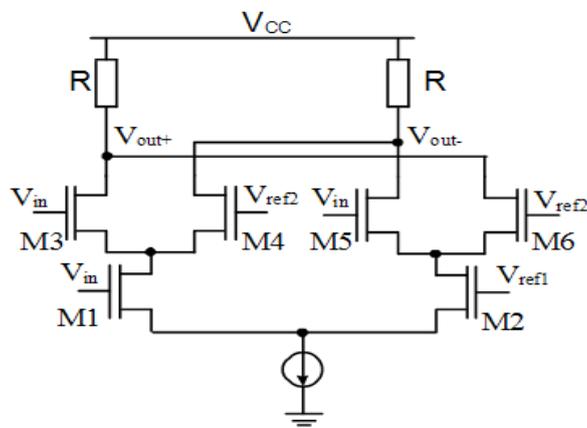


b)

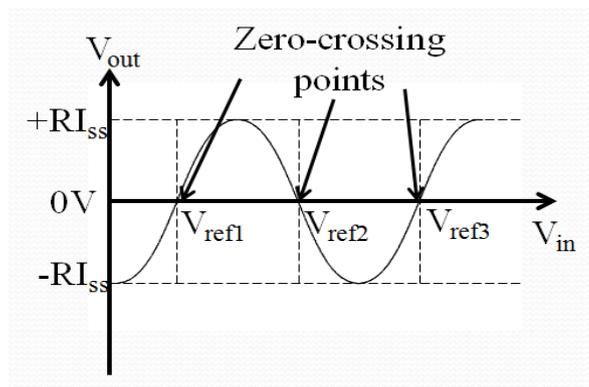**Fig. 2.** a) Cross-coupled differential pairs; b) Gilbert cell



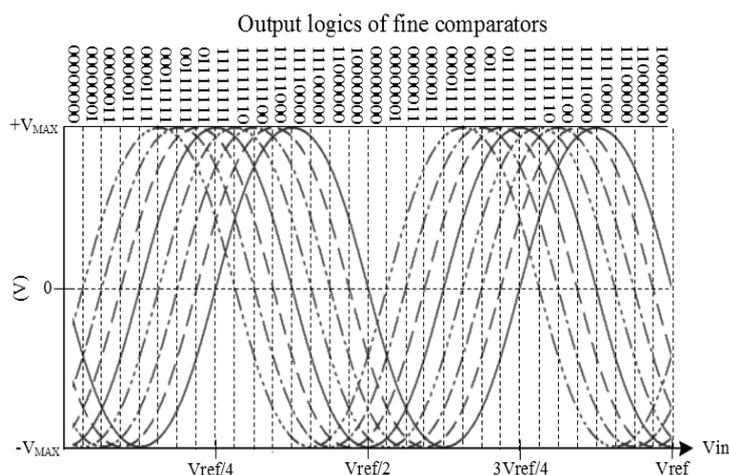**Fig. 3.** An output signal of a CCDP circuit with folding factor ($F_F$) = 3

**Fig. 4.** Output logics of fine comparators of a 3 fine bits folding ADC with zero-detection scheme

**Interpolating**

There are three types of interpolating circuits:

Resistive interpolating is the simplest interpolating circuit and consumes least power. Nevertheless, with an interpolating factor larger than two, interpolating signals are different in delay time.

Current interpolating uses current mirrors to overcome the difference in delay time between interpolating signals. However, it will increase power consumption, and since current mirrors suffer great mismatch, it also leads to low precision.

Active interpolating uses differential pairs to create interpolating signals. Although this increases the gain of the output signal and has the best linearity, power dissipation and hardware complexity will be higher than resistive interpolating.

Interpolating technique reduces the number of folding circuits to save the area and power consumption of ADC. On the other hand, the accuracy of interpolating signals depends on the overlap between linear ranges of folding signals and higher interpolating factor will also lead to lower accuracy. Therefore, a trade-off between accuracy and power dissipation has to be made when designing a folding ADC. Though the problem in the linearity of folding signals has been solved, there is still another problem in the folding factor which will be avoided by cascaded folding technique.

**Cascaded folding and pipelining**

The idea of cascaded folding technique is to use many folding stages to achieve high folding factor. Fig. 5 shows a cascaded folding circuit with a total folding factor is 9. Cascaded technique makes folding ADC architecture more flexible, and another advantage is the pipelining technique can be easily integrated to improve the performance of the system as shown in Fig 6. Without pipelining, the settling time from the first folding stage to the last folding stage must be within a clock cycle, while with pipelining, the settling time requirement of each stage is a half clock cycle. Thus, pipelining technique not only helps reduce the power consumption of the system but also increase the speed of a cascaded folding ADC.
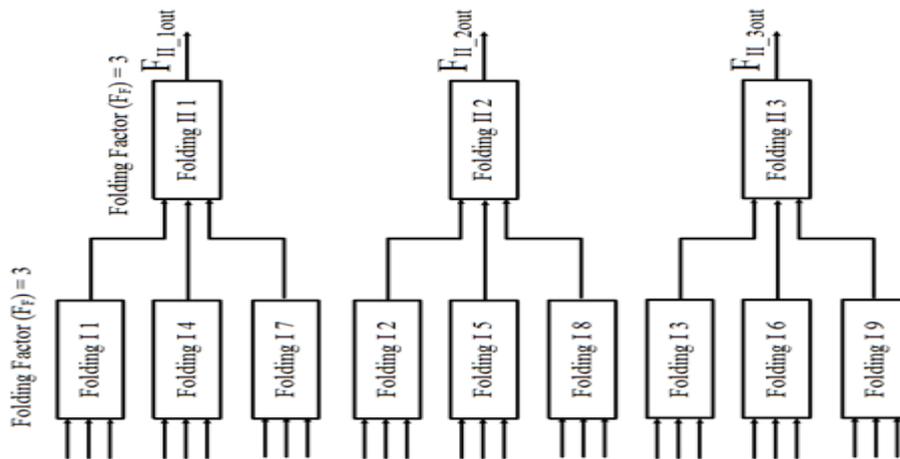
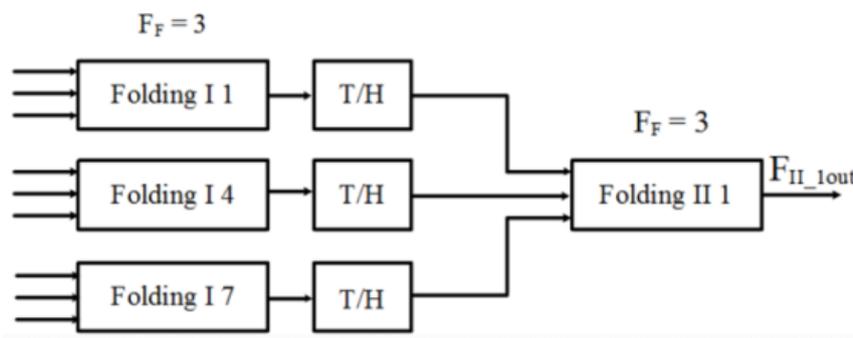**Fig. 5.** A cascaded folding circuit with a total folding factor is 9.



**Fig. 6.** A pipelined cascaded folding circuit.

## METHODS

### Design of ADC

From all the techniques have been discussed above, a 10-b 100 MS/s folding ADC is designed in a 0.18 μm technology with 1.8V power supply. Fig. 7 shows the block diagram of the designed ADC. The ADC has 5 coarse bits and 5 fine bits. To reduce noise, all analog signals in the ADC are differential. Input voltage range is 1.6 V. Folding circuits are also used in the coarse bits quantizer to further reducing the number of comparators. After three folding stages, input signal will be folded 40 times. Next, 32 fine comparators are used to detect zero-crossing points from 32 folding signals. Bubble error suppression circuits [2] will suppress bubble errors from output signals of the comparator blocks. Then, the encoder [2] will encode this signal to 5 fine bits. Finally, the digital correction will ensure the synchronization between coarse bits and fine bits; otherwise, there will be large errors in the output data of the ADC.
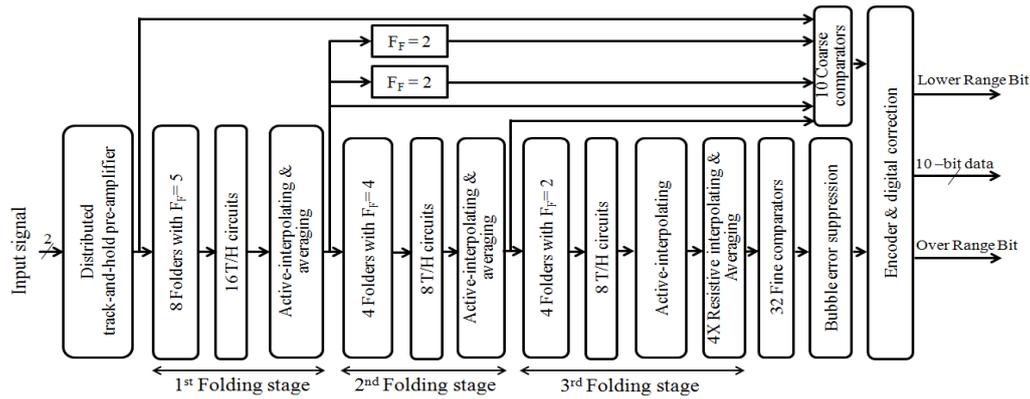
**Fig. 7.** Block diagram of the designed ADC

**Distributed T/H Pre-amplifier**

Performance of the T/H stage will mainly determine the performance of the ADC. In this design, distributed T/H pre-amplifier is used instead of a single costly T/H circuit. As pointed out in [4], this has many advantages such as higher linearity, better dynamic performance, lower power consumption and smaller area. However, two disadvantages of this method are the feed-through from the input signal through parasitic capacitance of differential pairs to reference voltage ladder, which can be solved by using small value resistors or decoupling technique in the reference ladder and differential pairs, and the difference in sampling time between T/H circuits.

Folding circuits in the first folding stage use CCDP circuits integrated with active interpolating circuits to reduce the number of pre-amplifiers. Other folding stages will use Gilbert cell as folding circuits. The T/H stage is depicted in Fig. 8 and the schematic of a pre-amplifier is shown in Fig. 9. Bandwidth (BW) of a pre-amplifier is calculated as:

$$BW = \frac{1}{\tau} = -\frac{1}{\pi T} \ln\left[1 - \frac{G}{A}\right]. \quad (1)$$

Where A is DC voltage gain, T is sampling clock period, and G is voltage gain at t = T/2. The reset switch will also be used in folding and active interpolating circuits. Hence, bandwidth of these circuits can still be calculated by (1).

**Averaging**

One of the main factors limits the resolution of high speed ADC is process variations. Averaging is a very effective method to improve DNL of the ADC. An averaging network with an infinite number of amplifiers is shown in Fig. 10. Comparing with other methods, averaging technique is simple, occupies small area and can easily be integrated with interpolating circuits. Therefore, a lot of researches into this technique have been made [5-10], [13]. Averaging networks can be implemented by using resistors or capacitors. Resistive averaging reduces mismatches between amplifiers, while capacitive averaging reduces mismatches in charge distribution between T/H circuits. Improving in offset voltage of a resistive averaging network is given in (2).
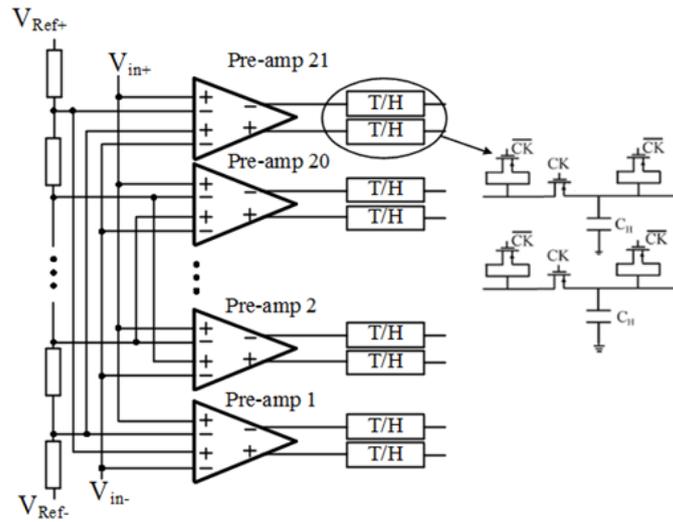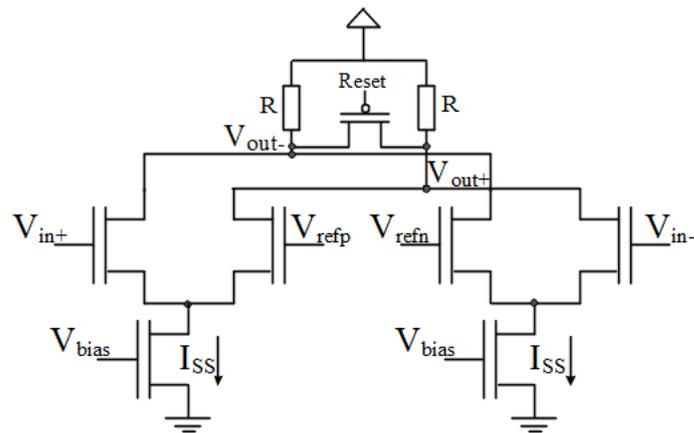
**Fig. 8.** Distributed T/H pre-amplifier
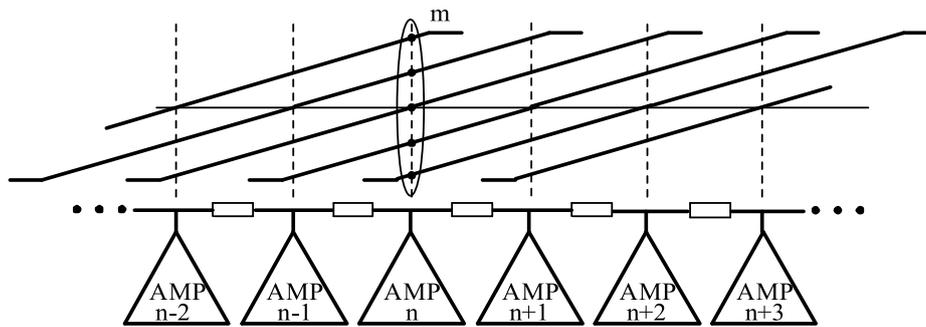


**Fig. 9.** Schematic of a pre-amplifier



**Fig. 10.** An averaging network with an infinite number of amplifiers

$$\frac{V_{offset}}{V_{offset-avg}} = \sqrt{1 + 4\left(\frac{R_{out}}{R_{eq}}\right) + 2\left(\frac{R_{out}}{R_{eq}}\right)^2} \qquad (2)$$

$$R_{eq} = \frac{R_{av}}{2} + \frac{\sqrt{R_{av}^2 + 4R_{av}R_{out}}}{2} \qquad (3)$$

Where $V_{offset}$ and $V_{offset-avg}$ are offset voltages before and after averaging, respectively, $R_{av}$ is the value of one resistor in averaging networks, and $R_{out}$ is the output impedance of an amplifier. If the ratio $R_{av}/R_{out}$ is small, the effect of the averaging network on amplifiers will be greater. However, the voltage gain of amplifiers will also be reduced. Since averaging networks are implemented after active interpolating circuits. Cross-coupled PMOS loads will be used to improve the voltage gain of active interpolating circuits. The output impedance is calculated as given in (4), where gm is the transconductance of MOSFET.

$$R_{out} = \frac{1}{g_{m5,8} - g_{m6,7}} \qquad (4)$$

In practice, the number of amplifiers is not infinite. Hence, amplifiers at the two ends of an averaging network will suffer boundary effect which leads to high systematic DNL and INL.

The increasing of the number of amplifiers in the linear region at the same time will increase the efficiency of averaging networks. In contrast, this will also increase the number of dummy amplifiers which are used to overcome the boundary effect at the two ends of averaging networks. Thus, the input voltage range will become smaller. However in this ADC, the boundary effect is eliminated by configuring averaging networks in mobius band. In addition, dummy zero-crossing points are also used at the two ends of the input voltage range. For this reason, the folding factor of the ADC is 40 instead of 32. Through simulation, there is no boundary effect in the input voltage range.

**Encoder and digital error correction**

The encoder in [2] is used to encode 31-b cyclic code to 5-b gray code. One folding signal won't be used in the encoder. That is the signal has the same form as the sixth bit (bit 5) of the designed ADC as shown in Fig. 11. Thus, it will be used to encode the sixth bit, convert 5-b gray code to binary and synchronize the remaining 4 coarse bits with fine bits. The synchronization scheme in [8] utilizes previous folding stages to reduce the number of coarse comparators.
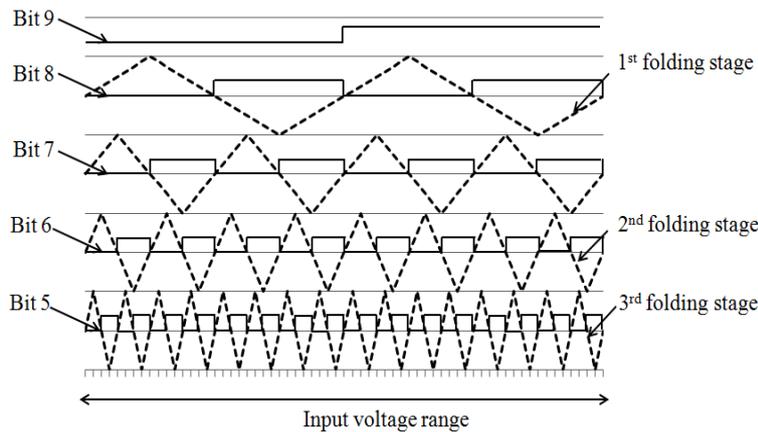


**Fig. 11.** Output signal forms from each stage of the designed ADC

Fig. 12 shows the synchronization scheme between the sixth bit (bit 5) and the seventh bit (bit 6) of the designed ADC. The logic function of bit 6 is $B6 = \overline{B5}.X1 + B5.X2$. The m block in Fig. 13 is the combinational logic circuit that executes this function. As shown in Fig. 11, output signals of the second folding stage have the same form as bit 6. Thus, synchronizing signals, X1 and X2 can be easily generated from two folding circuits of the second folding stage. After bit 6 has been synchronized, it will be used to synchronize bit 7. This will be repeated until bit 9 is reached as shown in Fig. 13. Synchronizing signals of bit 7 will be created from two extra folding circuits and synchronizing signals of bit 9, lower range and over range bits will be generated from pre-amplifiers.
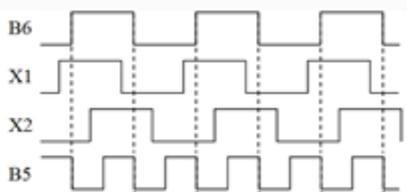


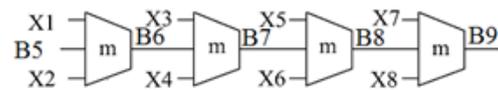**Fig.12.** The synchronization scheme between bit 5 and bit 6



**Fig. 13.** The synchronization circuit.

Note that, since pipelining technique is used, synchronizing signals are still needed to synchronize in the time domain with fine bits. This can be done easily by using D flip-flops to delay these signals.

**RESULTS**

Monte Carlo local simulation is used to estimate effects of process variations on DNL and INL of the ADC. Parameters changed are $V_{TH}$, $t_{ox}$, width and length of MOSFET. After 50 iterations, simulation results show that DNL is lower than 0.5 LSB, however, the INL is quite unacceptable for applications that need high precision. The DNL and INL simulation results are shown in Fig. 14.
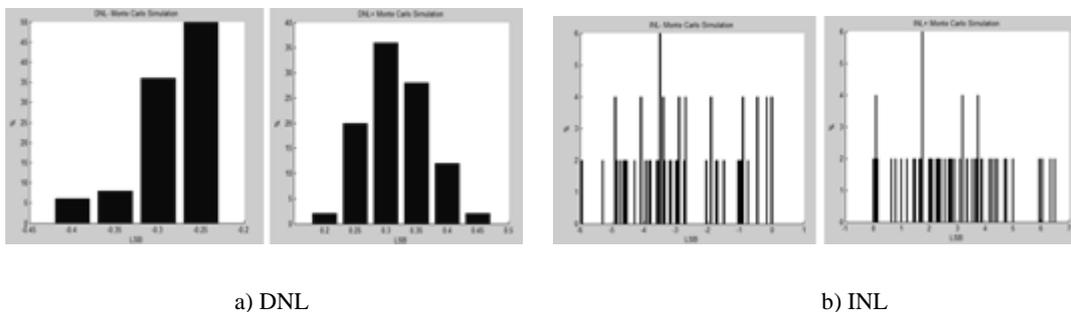


a) DNL                                  b) INL

**Fig. 14.** Monte Carlo simulation results

**Table 1.** Dynamic Performance Simulation Results

|       | SS       | TT       | FF       |
|-------|----------|----------|----------|
| Power | 63 mW    | 66 mW    | 67 mW    |
| SNR   | 54.98 dB | 59.18 dB | 59.03 dB |
| SFDR  | 60.9 dB  | 64.6 dB  | 64.68 dB |
| SNDR  | 53.67 dB | 57.6 dB  | 57.67 dB |
| ENOB  | 8.62-b   | 9.28-b   | 9.28-b   |

Table 1 shows dynamic performance simulation results at three corners SS, TT and FF with a 49 MHz input frequency. Fig. 15 shows the spectrum of the output signal at TT corner. At SS corner, the ADC still maintains the effective number of bit higher than 8-b. At TT and FF corners, simulation results are quite good; ENOB is above 9-b.

Fig. 16 shows the layout of the designed ADC. The ADC area after layout is 1.2 mm$^2$. Fig.

17 shows ENOB versus input frequency of the ADC with pre and post layout simulations. Large voltage drops on power supply wires and large parasitic capacitances on important signal wires cause great effect on the performance of the ADC.

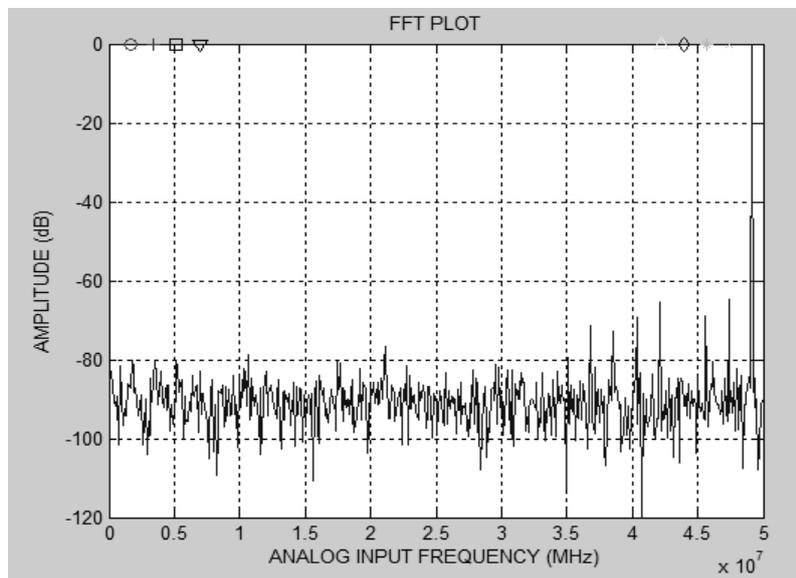Therefore, the effective resolution bandwidth (ERBW) of the ADC after layout is about 29 MHz.



**Fig. 15.** FFT 1024 points of the output signal with 49 MHz intput signal
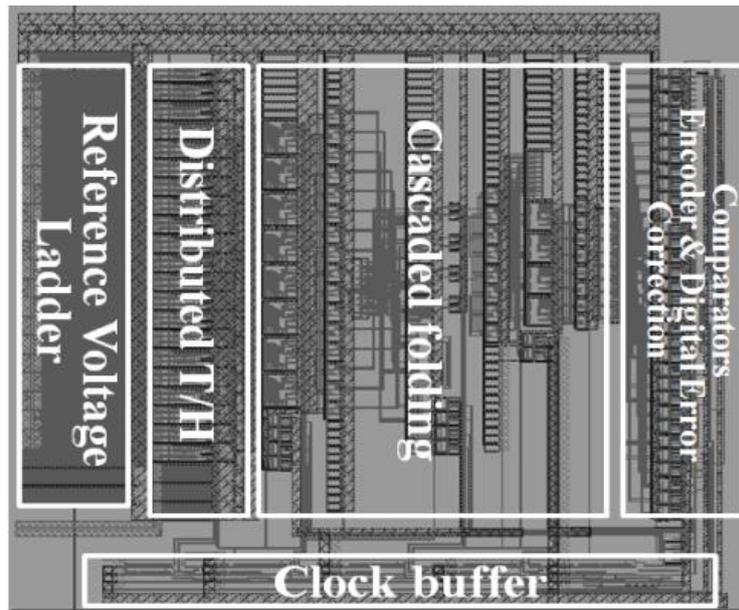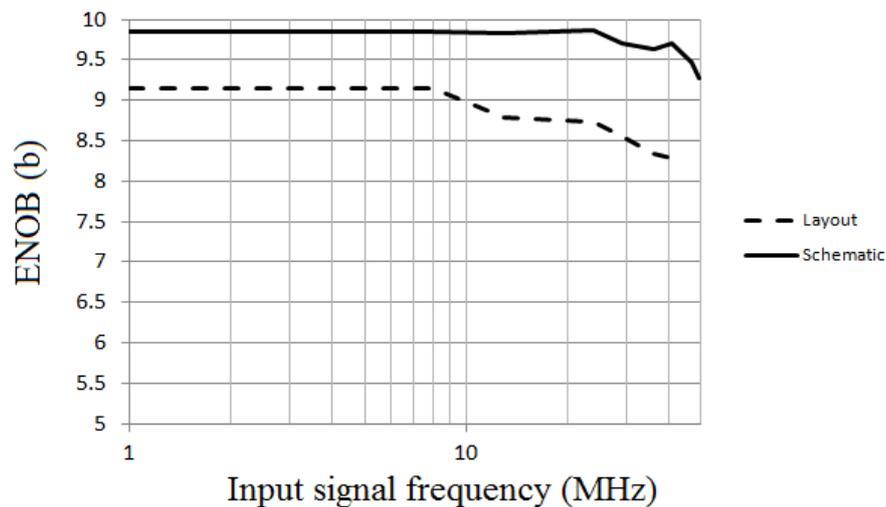
**Fig. 16.** Layout of the designed ADC



**Fig. 17.** ENOB versus input frequency

**CONCLUSION**

This paper presents a design of 10-b 100 MS/s folding ADC. By using distributed T/H preprocessing circuit and pipelining technique, performance of the ADC is improved and it only consumes 66 mW at TT corner. The effect of process variations on ADC performance is also estimated by Monte Carlo simulation. It can be concluded that averaging networks are very effective in reducing DNL error. However, for high precision applications, other offset compensation techniques will need to be used, e.g. self-calibration technique, to achieve better INL and ENOB. System architecture has been verified by pre and post layout simulations.

# Thiết kế mạch Pipelined Folding ADC 10-b tốc độ 100-MS/s sử dụng mạch tiền xử lý dò và giữ mức phân tán

- **Lê Bình Sơn**
- **Bùi Trọng Tú**
  Trường Đại học Khoa học Tự nhiên, ĐHQG-HCM
- **Lê Đức Hùng**
  Trường Đại học Điện tử – Thông tin, Nhật Bản

## TÓM TẮT

Bài báo này trình bày một mạch ADC 10-b được thiết kế ở công nghệ CMOS 0.18-µm. Để đạt được độ phân giải trên, kỹ thuật cascaded folding được sử dụng ở cả mạch chuyển đổi tinh và thô. Đồng thời, các tầng folding cũng được kết nối với nhau bằng kỹ thuật pipeline để giảm công suất tiêu thụ và duy trì tốc độ lấy mẫu 100-MS/s. Nhằm tận dụng kiến trúc vòng hở của kỹ thuật folding, mạch dò và giữ mức phân tán cũng được sử dụng, từ đó nâng cao hiệu suất của mạch. Các kết quả mô phỏng cho thấy, với tín hiệu vào là sóng sin ở tần số 49 MHz, thiết kế này đạt được 9.28 ENOB (effective number of bit) và công suất tiêu tán là 66 mW. Kết quả mô phỏng Monte Carlo cho thấy DNL thay đổi trong khoảng từ ±0.45 LSB tới ±0.25 LSB. Diện tích của mạch ADC sau khi layout là 1,2 $mm^2$.

**Từ khoá:** CMOS, ADC, folding, tốc độ cao

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