The modified space vector PWM for three-phase voltage source inverter with AC decoupling circuit

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ABSTRACT

This paper proposes the modified space vector pulse width modulation (SVPWM) control algorithm for the three-phase voltage source inverter (VSI), which consists of traditional six switches VSI and three bidirectional switches for creating the ac decoupling circuit. This topology has some advantages such as the ability to reduce the leakage ground current from PV panel and therefore improve the efficiency of photovoltaic (PV) energy conversion based on the principle of decoupling when the zero space vectors occur. Likewise, no current flows through six traditional switches in zero space vectors, thus they operate at lower average temperature. In this case, the conduction losses are reduced. For avoiding shoot-through states between six traditional switches and three bidirectional switches, a delay time has been added to switching time and managed carefully to guarantee THD of output voltage. Operating of the inverter with the modified SVPWM method is simulated by using Matlab/Simulink software and implemented in the experimental prototype by using FPGA Virtex 5 (Xilinx).

Keywords: *Heric converter, Deadtime, SVPWM, DSP, FPGA*

1. INTRODUCTION

Nowadays, conventional three-phase voltage source inverter (CVSI) is widely used in industrial and energy system, in order to convert electrical energy from DC to AC (Fig.1). This scheme is particularly applied in the electric motor drive systems and renewable energy systems such as photovoltaic (PV), fuel-cell conversion systems. The recent study on improving the efficiency of three-phase inverters is based on the structural changes of the VSI, therefore the principal scheme and control method for generating pulse patterns become more complex and it is difficult to be implemented for the existing VSI [1,2].

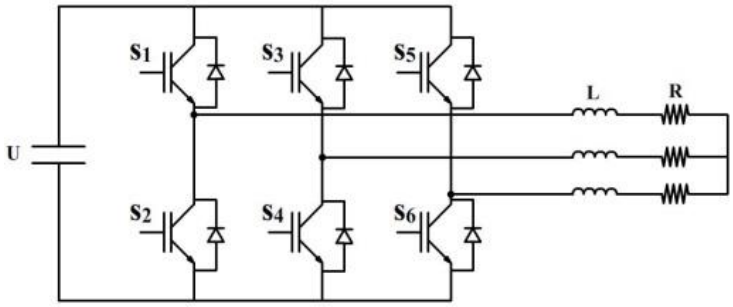
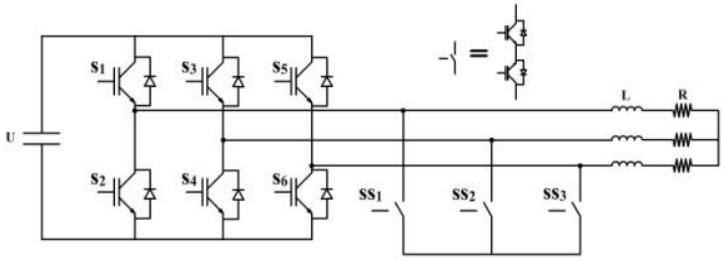
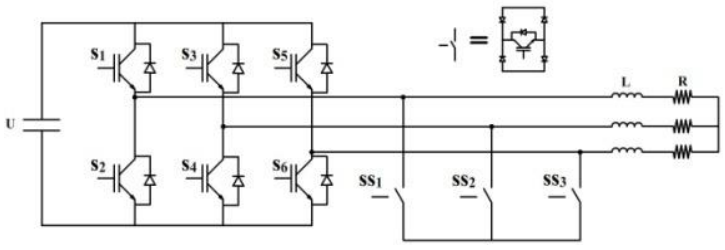


Figure 1. Conventional three-phase voltage source inverter

Recently, many research papers have been published for single-phase VSI scheme for transformerless grid-connected system. The efficiency improvement is based on the principle of AC or DC decoupling, when zero state occurs. In these works, some topologies, based on the H-bridge with an AC bypass circuit consisting of a bidirectional switch (HERIC topology) [3] or a diode rectifier and a switch with clamping to the DC midpoint (HB-ZVR topology) [4], are proposed. In case of DC decoupling circuit, some topologies are invented, which consists one extra switch (H5 topology) [5] or two extra switches (H6 topology) [6,7]. High conversion efficiency in these schemes is obtained.



a) Decoupling circuit with three bidirectional switches



b) Decoupling circuit with three diode rectifier and switches

Figure 2. Proposed high efficient three-phase voltage source inverter with AC decoupling circuit (MVSI)

However, this principle has not been analyzed and applied for three-phase inverters in more details. In order to increase the efficiency, the proposed schemes usually pay attention to the use of multilevel principles [8,9]. This leads to a change in configuration and availability of PWM methods such as SVPWM of the well-developed three-phase two-level VSI.

This paper analyses the topology of modified three-phase VSI (MVSI), which consists of traditional six switches voltage source inverter and three bidirectional free-wheeling switches for creating the AC decoupling circuit as shown in Figs. 2a and 2b.

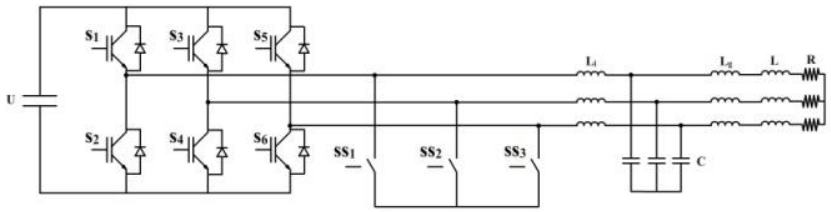


Figure 3. MVSI with an output LCL filter

This topology has some advantages such as the ability to improve the efficiency based on the principle of decoupling, the ability of applying to the CVSI scheme, the simplicity of the control algorithm (modified SVPWM) and can widely applied to many applications.

This topology can be applied to: The application of electrical energy conversion from DC to AC:

- For providing the AC voltage with fixed frequency and effective value to the load (such as RL load) with the output LCL filter for obtaining the true sinusoidal waveform (Fig. 3).
- For providing the AC voltage with variable frequency and variable effective value to the load (such as induction motor), without the output LCL filter (Fig. 2a, 2b).

Fig.4 shows the PV panels three-phase grid-connected applications with an isolation low voltage transformer. Almost the network configurations are divided into two groups: with galvanic isolated transformer and transformerless. The grid connected configuration with isolated transformer has advantages such as safety, no leakage current, no DC current injection. In contrast, transformerless topology has higher efficiency, but it has more complex control algorithms and some related issues such as leakage current and DC current injection into the grid.

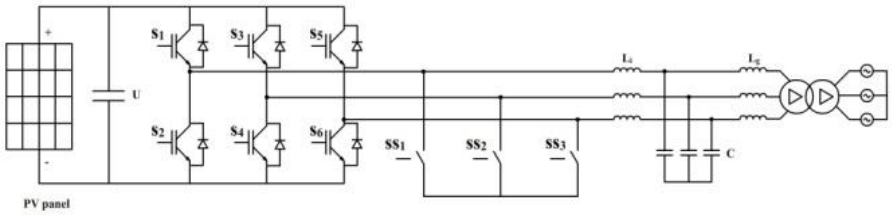


Figure 4. MVSI PV grid-connected system

2. PROPOSED MODIFIED THREE-PHASE VOLTAGE SOURCE INVERTER TOPOLOGY AND DEAD TIME GENERATION ALGORITHM

A. Structure and principle of the MVSI

Proposed topology, called the MVSI, uses a modified topology of the three-phase bridge VSI, by adding an AC-decoupling circuit, which composes of three extra bidirectional switches with two options as shown in Fig. 2a and 2b.

The principle of the MVSI scheme is the isolation of AC output from DC-link input when the zero space vector occurs (S1, S3, S5 are ON or S2, S4, S6 are ON in CVSI scheme). The output current of the proposed configuration flows in a path with AC decoupling circuit via three extra freewheeling switches (SS1 to SS3) and therefore the energy consumption of DC-link is reduced, i.e. increasing the efficiency of inverter.

Semiconductor losses in VSI can be calculated by using the method in [10]. The efficiency of the VSI and proposed MVSI is calculated as follow:

$$\eta = \frac{P_{out}}{P_{in}} \quad (1)$$

where P_{in} is the input DC power, P_{out} is the ouput AC power according to 1st voltage harmonic:

$$P_{in} = V_{dc} I_d \quad (2)$$

$$P_{out} = 3V_{1RMS} I_{1RMS} \quad (3)$$

B. Modified Space Vector PWM algorithm for the MVSI

The SVPWM is based on the formation of three voltage vectors in sequence in one sampling interval T_s so that the average output voltage meets the requirement. In the SVPWM method for the VSI, there are six active vectors and two zero vectors. The reference output vector is synthesized by using two active vectors and one zero vector. The active and zero vector of each sector in conventional algorithm are shown in Fig. 5.

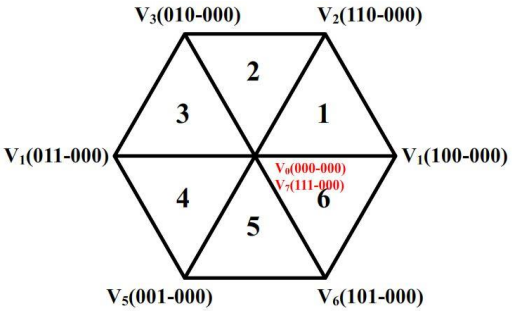


Figure 5. Space vectors of CVSI.

The calculations of the duration of two active and two zero vectors are as follows for a half of sampling period [11].

$$T_x = \frac{\sqrt{3}}{\pi} M T_s \sin(\frac{\pi}{3} - \alpha)$$
$$T_y = \frac{\sqrt{3}}{\pi} M T_s \sin(\alpha) \quad (4)$$
$$T_z = \frac{T_s}{2} - T_x - T_y$$

where: T_x – duration for vector active vector V_x, T_y – duration for active vector V_y, T_z – duration for zero vector V_z (included V_0 and V_7), M – modulation index M = V^*/V_{1sw} (V^* - amplitude of the reference voltage vector, V_{1sw} – peak value of six-step voltage).

Based on the analysis of SVPWM, the modified space vector PWM is proposed in this paper. The difference of this modified SVPWM from the conventional one is when the zero space vector (ZV) occurs, in the proposed

topology (MVSI), all switches SS_1, SS_2 and SS_3 are turned on and all S_1, S_2, S_3, S_4, S_5 and S6 are turned off. This way, using SS_1 – SS_3 as shown in Figs. 2a and 2b, the zero-voltage space vector is realized by short-circuiting the output of the inverter, during which period the DC-link is separated from the load or the grid, because all switches S_1 – S_6 are turned off. Three voltage vectors of each sector in modified algorithm are shown in Fig. 6.

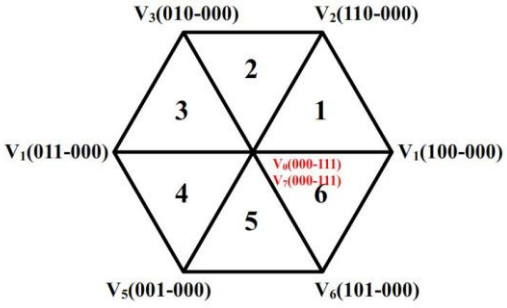


Figure 6. Space vectors of MVSI

However, the dead-time interval (DTI) should be applied between switching states of the main switches (S_1 to S_6) and bidirectonal switches (SS_1 to SS_3) to avoid short-circuit state. When the zero space vector occurs, six main switches are turned off instantly and three bidirectional switches are turned on after a while. When the zero space vector finishes, three bidirectional switches are turned off instantly and six main switches are turned on after a while. This interval is called dead time. The flowchart of this algorithm is shown in Fig. 7.

For the modified algorithm, there are two switches which are turned off completely in each sector which is shown in Table 1. However, in the dead-time interval where no switch is turned on, so the current will flow through the free-wheeling diode and the output voltage can not be controlled. This state is called off-state and can distort the output voltage and current, which effect to the power quality. The switching states in the sector 1 are shown in Fig. 8.

TABLE 1. INACTIVE SWITCHES OF EACH SECTOR

Sector	**1**	**2**	**3**	**4**	**5**	**6**
Inactive switches	S2 S5	S4 S5	S4 S1	S6 S1	S6 S3	S2 S3

This modified SVPWM is very simple and easy to implement by using a FPGA controller for generating switching patterns.

C. The proposed SVPWM and Dead-time Generation algorithms for the MVSI

In order to improve the quality of output voltage and current, the above algorithms needs to be changed. At any time, at least two switches must be turned on. This can be implemented in three states, so this algorithm can be called three-stage dead-time generation algorithm. If there are only two switches which are turned on, this is called two-switch state. If there are two above switches and three bidirectional switches which are turned on, this is called five-switch state. The last state is zero state or modulation state in which there are three switches or bidirectional switches turned on.

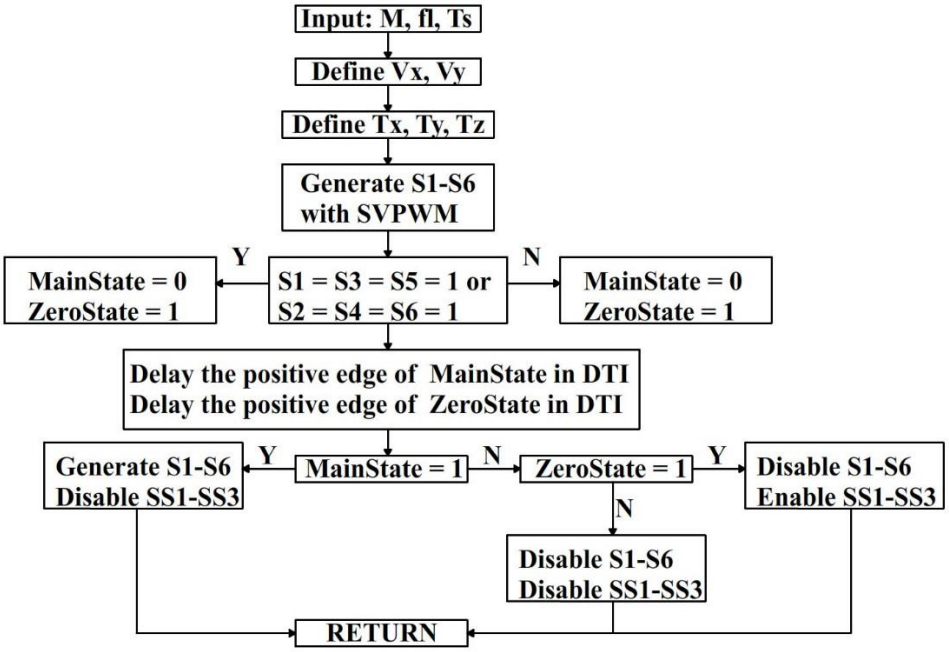


Figure 7. Flowchart of the modified SVPWM algorithm

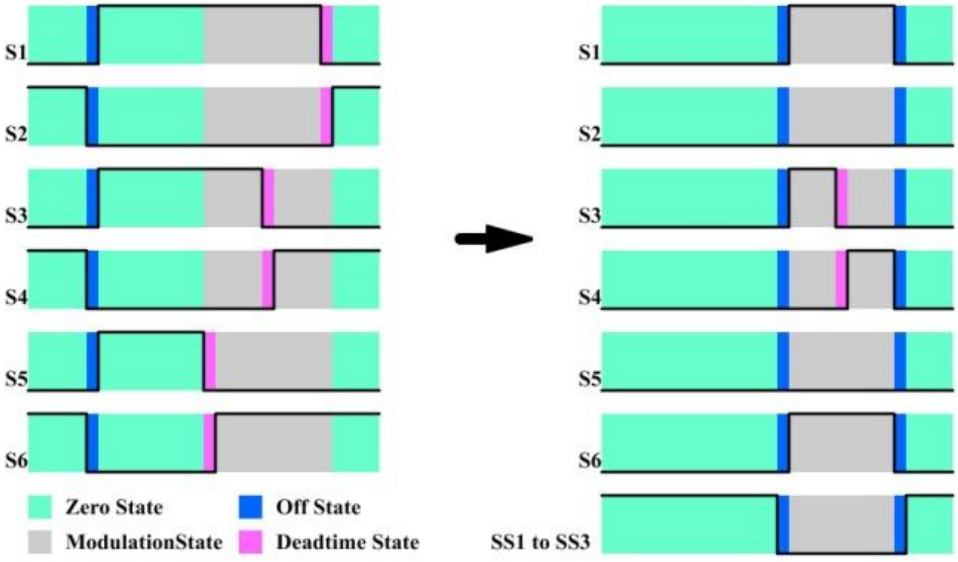


Figure 8. Switching process of modified algorithm when ZV occurs and finishes in sector 1

When the zero space vector begins, two switches which according to each sector are kept turning on to create two-switch state. After a while, three bidirectional switches are turned on to create five-switch state. At last, two above switches are turned off and the AC-side is

separated from DC-side completely, this is the zero state.

When the zero space vector finishes, two switches which according to sector were turned on before a while to create five-switch state. Then, three bidirectional switches are turned off to create two-switch state and the inverter is in the modulation state.

The inactive switches of each sector are similar to the one of the modified algorithm and the active switches which must be turned on for a while are shown in Table 2. The flowchart of the proposed algorithm is shown in Fig. 9 and the switching state of sector 1 is shown in Fig. 10. As shown in Fig. 10, the problem which is mentioned in the modified algorithm is solved; the off-state is removed completely.

The proposed algorithm is more complex than the modified algorithm, so it is difficult to implement on DSP because it needs to be implemented on a fast microprocessor. Fortunately, everything can be done with FPGA technology.

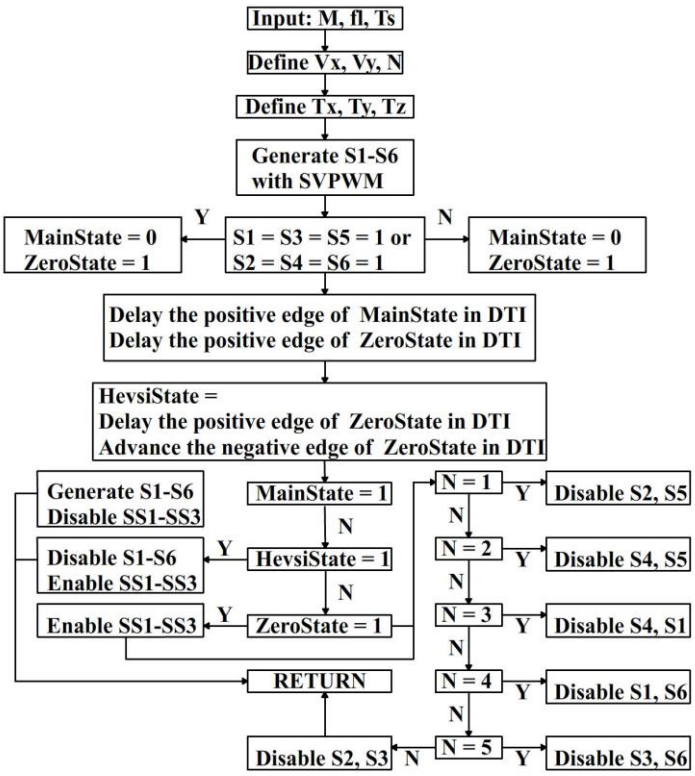


Figure 9. Flowchart of the proposed SVM algorithm

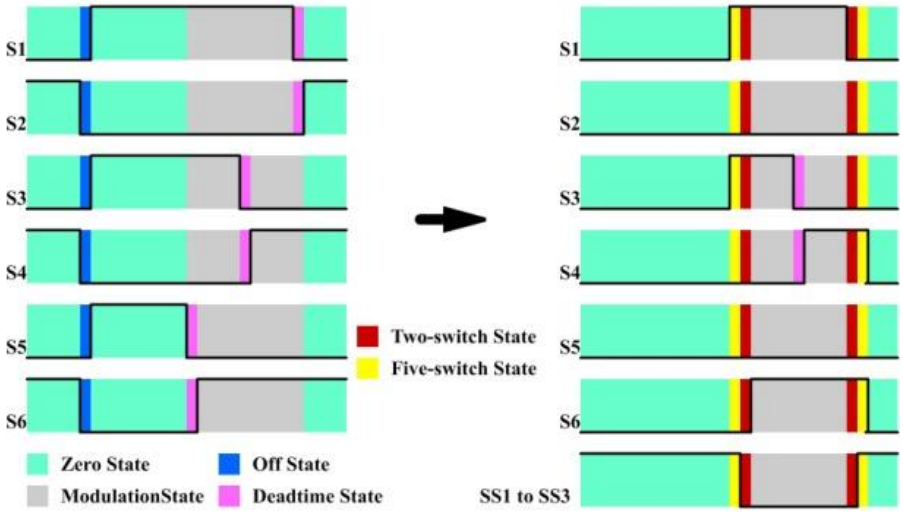


Figure 10. Switching process of proposed algorithm when ZV occurs and finishes in sector 1

TABLE 2. ACTIVE SWITCHES OF EACH SECTOR

Sector		**1**	**2**	**3**	**4**	**5**	**6**
Active switches	***ZV begins***	S4 S6	S2 S6	S2 S6	S2 S4	S2 S4	S4 S6
	ZV finishes	S1 S3	S1 S3	S3 S5	S3 S5	S1 S5	S1 S5

3. SIMULATION OF THE PROPOSED SVPWM ALGORITHM

The simulation model is implemented in Matlab/Simulink with SimPowerSystem Toolbox, which is shown in Fig. 11. The parameters of the simulation model are given as follows:

- DC-link voltage: U = 600V
- Switch parameters: IGBT resistor on = 0.02Ω, IGBT forward voltage = 2.5V, Diode resistor on = 0.01Ω, Diode forward voltage = 0.8V
- Leakage capacitor = 10nF
- Load: R = 5 – 8 – 13 – 27Ω (corresponding to 20 – 15 – 10 – 5kW), L = 10mH, star-connected
- Reference output: U = 380V (line-to-line), f = 50Hz
- Basic voltage U_{base}=311V, Basic power P_{base}= 10kW
- Proposed SVPWM: switching frequency f_{sw}=10kHz, dead-time interval TDI= 1 µs

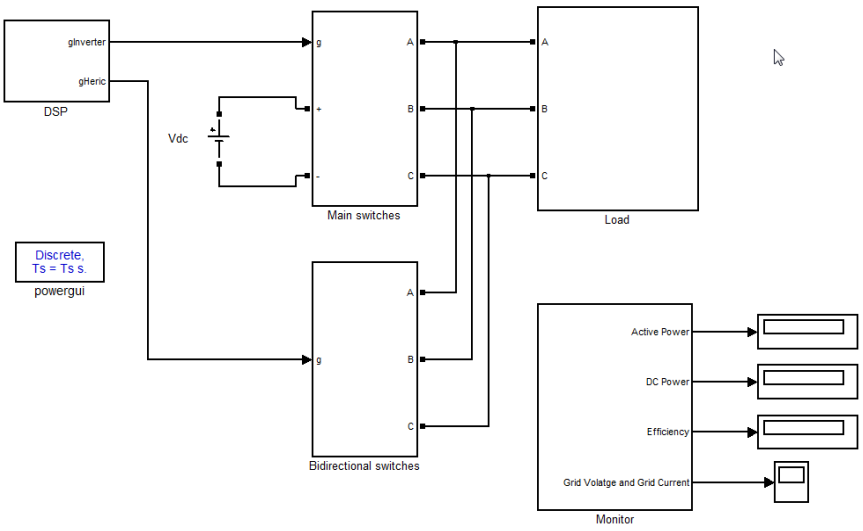
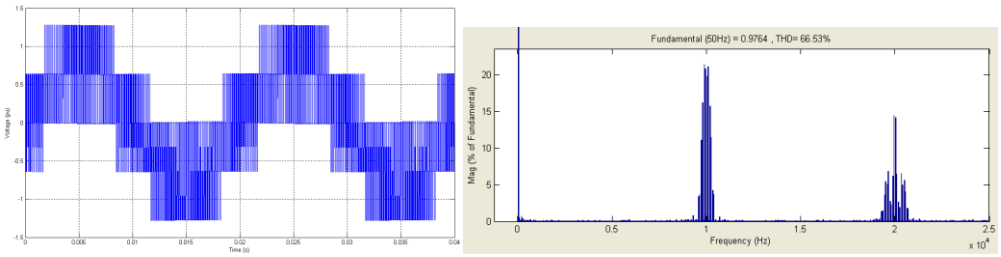
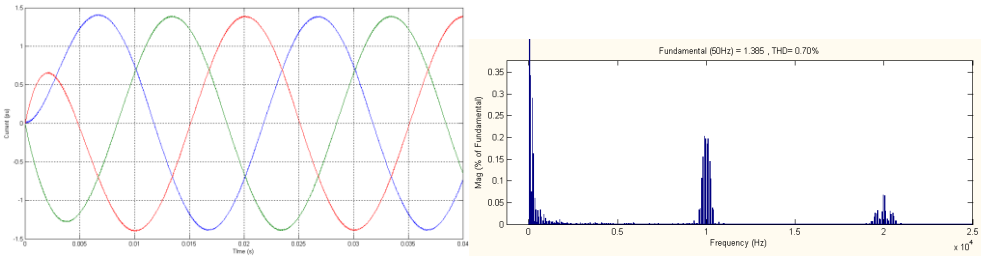


Figure 11. Simulation model of MVSI

The load voltage/current of the case 20kW, the input/output power and the leakage currents are shown in Figs. 12, 13, 14, respectively. The simulation results of other cases are expressed in Tables 3 and 4.



(a) Load voltage: Fundamental harmonic peak = 0.9746 pu THD = 66.53%



(b) Load current: Fundamental harmonic peak = 1.395 pu THD = 0.7%

Figure 12. Simulation results of a) Phase output votlage and its FFT analysis
b) Three-phase output current and its FFT.

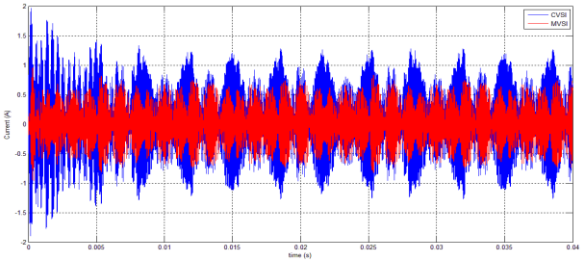


Figure 13. Leakage current responses

It can be seen that the efficiency of MVSI is higher than CVSI. Fig. 15 shows the efficiency comparison of CVSI and MVSI according to the output power. Otherwise, the leakage current of MVSI is lower than CVSI.

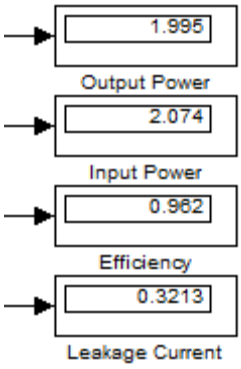


Figure 14. The output/input power, the corresponding efficiency and the leakage current of the proposed converter.

TABLE 3. SIMULATION RESULTS OF CVSI

Load type (kW)	**Input power (pu)**	**Output power (pu)**	**Efficiency (%)**	**Load voltage (pu)**	**Voltage THD (%)**	**Current THD (%)**	**Leakage Current (A)**
5	0.560	0.4948	88.36	0.9643	70.41	2.58	0.5151
10	1.056	0.9833	93.08	0.9642	70.49	1.45	0.5173
15	1.549	1.467	94.69	0.9648	70.33	1.02	0.5223
20	2.046	1.952	95.39	0.9667	69.93	0.75	0.5213

TABLE 4. SIMULATION RESULTS OF MVSI

Load type (kW)	**Input power (pu)**	**Output power (pu)**	**Efficiency (%)**	**Load voltage (pu)**	**Voltage THD (%)**	**Current THD (%)**	**Leakage Current (A)**
5	0.560	0.5063	90.37	0.9756	66.71	2.47	0.2897
10	1.068	1.006	94.19	0.9752	66.80	1.36	0.3064
15	1.570	1.499	95.48	0.9753	66.73	0.95	0.3110
20	2.074	1.990	95.99	0.9764	66.53	0.70	0.3213

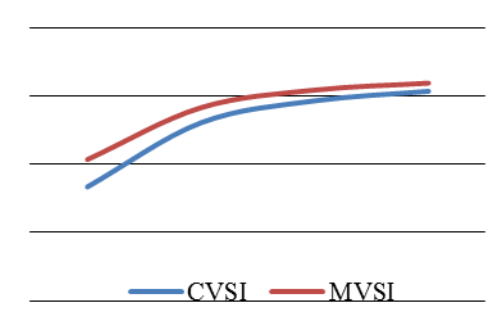


Figure 15. Efficiency characteristic versus power load (in kW)

4. EXPERIMENTAL OF THE PROPOSED SVPWM ALGORITHM

The labopratory prototype of the MVSI is shown in Fig. 16. The parameters of the experimental setup are:

- Switches: IGBT FGL60N100 (1000V, 60A)
- Microprocessor: FPGA Virtex 5 (Xilinx)
- Driver: Optocoupler HCPL 3020
- Load: R = 3.3Ω, L = 5mH, star-connected
- DC-link voltage: U = 130V
- Proposed SVPWM: modulation index M = 0.8, load frequency f_{out}= 50Hz, switching frequency f_{sw}= 10kHz, dead-time interval = TDI = 2µs

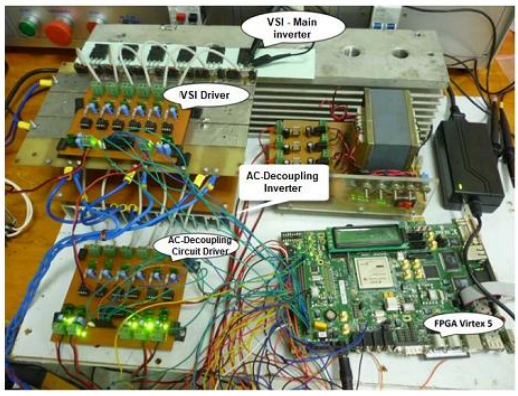
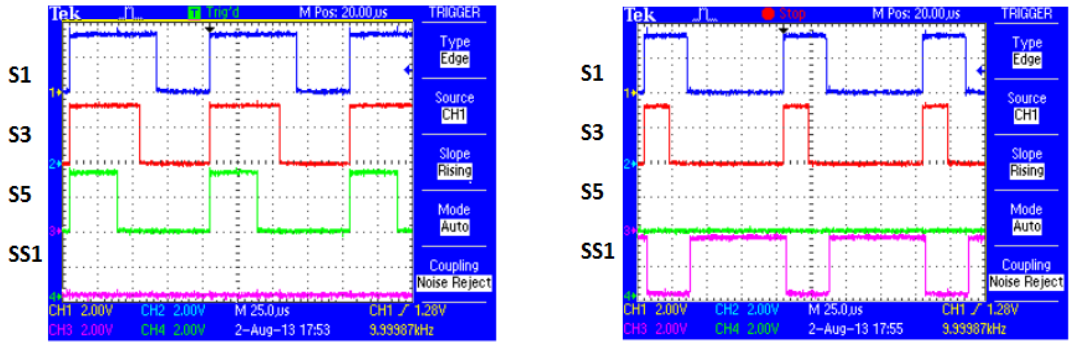


Figure 16. Experimental setup of MVSI

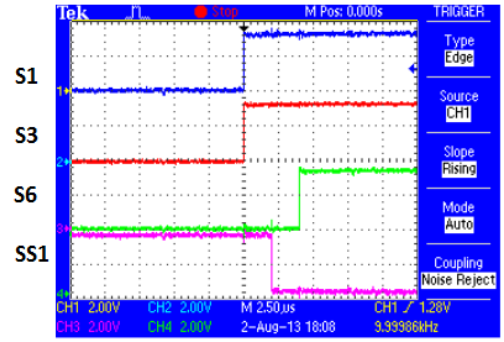
The switching pattern of sector 1 for the CVSI and MVSI is shown in Fig. 17. In CVSI, pulse SS1 is always turned off. In MVSI, the zero-state duration in which all three pulses of CVSI are 1 or 0, so the pulses of AC decoupling circuit will be turned on in this duration and all pulse of VSI will be turned off immediately. There are also switching steps between normal mode and high efficiency mode, which are mentioned in proposed SVPWM algorithm and are shown in Fig. 18.



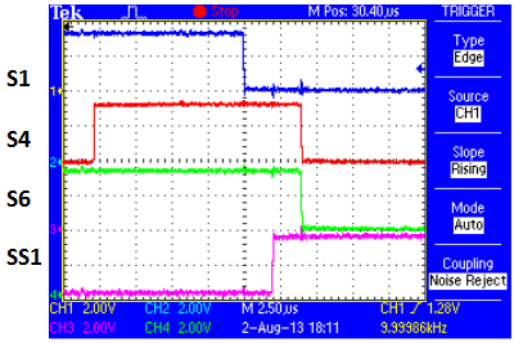
a) Switching pattern of CVSI

b) Switching pattern of MVSI

Figure 17. Experimental results of switching pattern in case a) CVSI b) MVSI



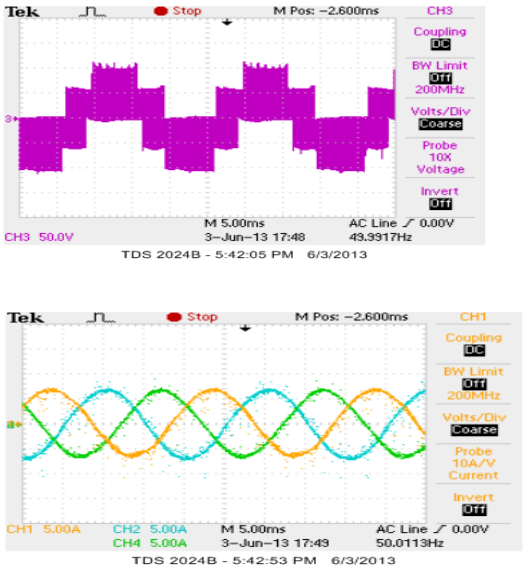
a) The zero state finishes



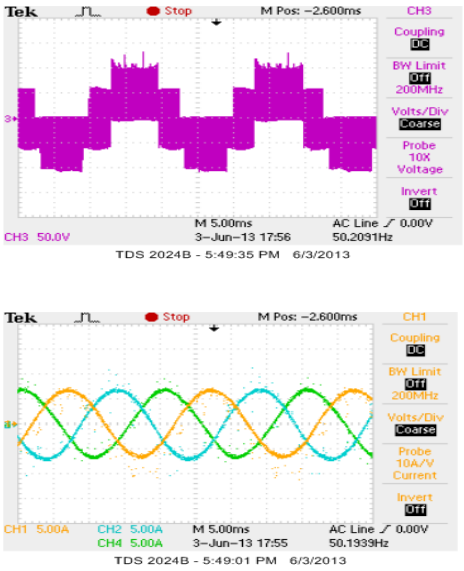
b) The zero state begins

Figure 18. Three-stage switching algorithm

The load voltage/current of CVSI and MVSI are shown in Fig. 19a and 19b, respectively. Table 5 and 6 provides some more experimental results in different condition. It is easealy seen that the MVSI provides the high efficiency as compare to the CVSI.



a) CVSI (CH1,2,4 : 5A/div; CH3 : 50V/div)



b) MVSI (CH1,2,4 : 5A/div; CH3 : 50V/div)

Figure 19. The experimental results of output voltage and current of a) CVSI b)MVSI

TABLE 5. EXPERIMENTAL RESULTS OF CVSI

DC voltage (V)	DC current (A)	Input power (W)	Output power (W)	Efficiency (%)
132.2	5.139	679.3758	629	92.5850
132.2	5.176	684.2672	635	92.8000
133.3	5.178	690.2274	636	92.1436
133.3	5.164	688.3612	637	92.5386
132.3	5.165	688.4945	640	92.9564
133.5	5.173	690.5955	640	92.6736
133.3	5.152	686.7616	633	92.1717
133.0	5.138	683.3540	630	92.1923
133.0	5.133	682.6890	629	92.1357
133.0	5.133	682.6890	629	92.1357
133.1	5.139	684.0009	632	92.3975
Average Efficiency (%)				92.4000
Average Temperature (°C)		***Main switches***		62.0400
		Bidirectional switches		28.3300

TABLE 6. EXPERIMENTAL RESULTS OF MVSI

DC voltage (V)	DC current (A)	Input power (W)	Output power (W)	Efficiency (%)
132.3	5.111	676.1853	628	92.8740
132.5	5.120	678.4000	630	92.8756
132.9	5.115	679.7835	632	92.9708
133.0	5.112	679.8960	634	93.2496
132.3	5.084	672.6132	622	92.4751
132.5	5.086	673.8950	625	92.7444
132.7	5.090	675.4430	626	92.6799
132.5	5.069	671.6425	626	93.2043
133.0	5.085	676.3050	627	92.7097
132.9	5.089	676.3281	626	92.5586
133.5	5.105	681.5175	635	93.1744
Average Efficiency (%)				92.9000
Average Temperature (°C)		***Main switches***		55.8300
		Bidirectional switches		38.3300

5. CONCLUSIONS

The topology of MVSI is proposed. The MVSI topology consists of conventional six switches two level VSI and auxiliary three bidirectional switches in order to create the AC decoupling circuit. The modified SVPWM with dead-time generation algorithm is also analysis. The proposed MVSI topology with MSPWM method is simulated by using Matlab/Simulink software. In order to validate the simulation results. An experimental prototype was built and the experimental shown that the high efficiency of the proposed MVSI is obtained very promising.

Acknowledgment

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Thuật toán điều chế độ rộng xung véc tơ không gian cải tiến cho bộ nghịch lưu áp ba pha với mạch cách ly phía xoay chiều

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TÓM TẮT

Bài báo này đề xuất thuật toán điều chế độ rộng xung vector không gian cải tiến (SVPWM) điều khiển cho bộ nghịch lưu áp ba pha (VSI), sơ đồ gồm sáu khóa bán dẫn truyền thống và ba công tắc xoay chiều để tạo mạch cách ly phía xoay chiều. Cấu trúc này có ưu điểm như khả năng làm giảm dòng rò đất từ các tấm pin mặt trời PV và do đó nâng hiệu suất chuyển đổi năng lượng quang điện (PV) dựa trên nguyên tắc cách ly ở thời điểm các vectơ không gian 0. Bên cạnh đó, không có dòng đi qua sáu khóa bán dẫn truyền thống ở thời điểm vectơ không gian 0, do đó chúng hoạt động ở nhiệt độ trung bình thấp hơn. Trong trường hợp này, các tổn hao dẫn các khóa này được giảm bớt. Để tránh trạng thái ngắn mạch giữa sáu khóa truyền thống và ba khóa xoay chiều khi chuyển mạch, một giá trị thời gian trễ đã được thêm vào thời gian chuyển mạch và được phân bố hợp lý để đảm bảo chất lượng của điện áp ngõ ra. Hoạt động của bộ nghịch lưu với phương pháp SVPWM cải tiến được mô phỏng bằng cách sử dụng phần mềm Matlab / Simulink và kiểm chứng trên mô hình thử nghiệm sử dụng card điều khiển FPGA Virtex 5 (Xilinx).

Từ khóa : *Bộ nghịch lưu Heric, Thời gian trễ, SVPWM, DSP, FPGA*

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