SIMULATION OF CURRENT-VOLTAGE CHARACTERISTICS OF SPIN FIELD EFFECT TRANSISTOR USING NEMO-VN2

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ABSTRACT: *We have developed a simulator for nanoelectronics devices, NEMO-VN2. In this work, we provide an overview of spin field effect transistor. We use the simulator to explore the performance of spin FET. The model of the spin FET is based on non-equilibrium Green function method and implemented by using graphic user interface of Matlab. The current-voltage characteristics such as drain current-voltage, drain current-gate voltage ones are explored.*

Keywords: *Spin transistors, spin FET, non-equilibrium Green function, drain current-voltage characteristics, drain current-gate voltage characteristics.*

INTRODUCTION

In recent years, a vigorous research effort to demonstrate spin transistors has been pursued. One of the motivations has been that spin transistors are identified as one of the most promising alternatives to traditional MOSFET by the International Technology Roadmap for Semiconductors [1]. Simulations have predicted that spin transistors can scale in their size with smaller switching energy and less overall power dissipation than MOSFET.

The idea of spin field-effect transistor sparked after Fert et al. [2] and Grunberg et al. [3] discovered the giant magneto resistance effect in magnetic multilayer systems in 1988. They found huge differences in current coming out of a magnetic and metallic multilayer system when the magnetic layers had the same or different scattering of electrons. Shortly thereafter room temperature magnetic field sensors were made [4] using spin property

which had much better performance than previously used anisotropic magneto resistance property.

Following the preliminary realization of the potential benefits of utilizing spin property, Datta and Das proposed an electron wave analog of the electro-optic light modulator in the late 1989 [5]. Most of the today's interest in this newly born field of study is motivated by their well-known proposed device which is now known as *spin field-effect transistor* (spin FET).

In this work, we start with an introduction to the concepts of electron spin and proposed spin field effect transistor in the first section. In the second section, we look more into details of spin field effect transistor from a device point of view (e.g. energy band diagram, device structures). Finally we discuss typical simulations of current-voltage characteristics in spin FET by non-equilibrium Green function

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method using graphic user interface (GUI) of Matlab.

OVERVIEW AND SIMULATION OF SPIN FET

Concepts of electron's spin

Spin of electron is a fundamental property which originates from electron's spinning around its axis. Depending on the direction of the angular momentum that this spinning causes we can call them spin-up ($\uparrow$) when the

angular momentum is pointed up or spin-down ($\downarrow$) when it is pointed downwards.

In giant magneto resistance effect which we mentioned shortly before, a huge change is observed in the amount of resistance facing current passing through a metal which is sandwiched between two ferromagnets. Namely, the following ratio for devices showing giant magneto resistance effect is huge.

$$GMR = \frac{R_{\uparrow\downarrow} - R_{\uparrow\uparrow}}{R_{\uparrow\uparrow}} \tag{1}$$

In this equation GMR represents giant magneto resistance ratio, $R_{\uparrow\downarrow}$ is the resistance of the device when polarization of ferromagnets are anti-parallel, and $R_{\uparrow\uparrow}$ is the resistance of the device when polarization of ferromagnets are parallel.

Tunneling magneto resistance yields three times bigger magneto resistance values at room temperature with respect to giant magneto resistance [6] and therefore it is a good choice in making room temperature electronic devices.

Considering the fact that this device can show a large or small resistance for anti-parallel or parallel orientations of the

magnetizations of ferromagnets, respectively, it can work as a valve and that is why this device is sometimes called s*pin valve*.

Datta and Das spin FET

In the late 1989 Supriyo Datta and Biswajit Das from Purdue University proposed an electron wave analog of the electro-optic light modulator [5]. Most of the today's interest in spintronics is motivated by their well-known proposed device which is now known as the spin field-effect transistor.

Datta-Das paper spurs new research direction. The operation of ideal Datta-Das spin FET can be sketched in Figure 1.
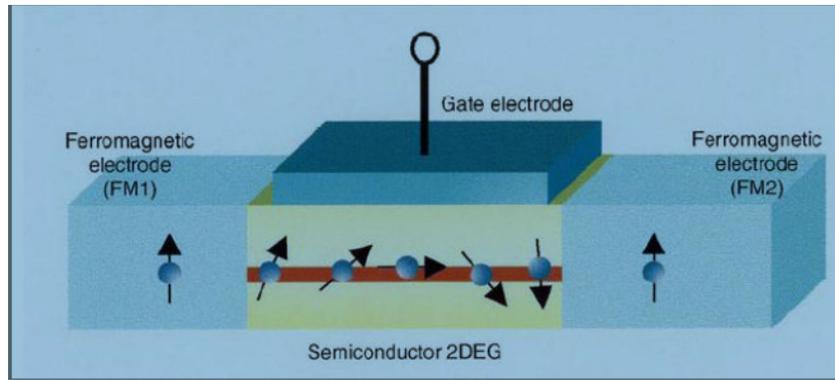
Figure 1. Basic configuration of a spin field-effect transistor proposed by Datta and Das.

Electric field is seen as B-field in electron rest frame and given by

$$B_{eff} = \frac{2m^*}{eh^2}\alpha E_y v = \frac{2m^*V_G}{eh^2 t_{ox}}\alpha v \qquad (2)$$

where B_{eff}, m^*, e, h, α, E_y, v, V_G, and t_{ox} are effective magnetic field, effective mass, electron charge, Plank constant, Rashba coefficient, electric field, drift velocity, gate voltage, and gate thickness, respectively. Electric field can induce precession of electron's spin in the semiconductor channel.

The spin direction of electrons can be manipulated by the gate voltage. The spin precession angle of the electrons in the semiconductor channel depends on the strength of applied voltage described by a phenomenon which is known as *Rashba effect*. The spin precession angle of electrons, $\Delta\theta$ is given by:

$$\Delta\theta = \frac{2m^*L_G}{\hbar^2}\Delta\alpha \qquad (3)$$

where, $\Delta\alpha$, L_G, and $\hbar$ are Rashba coefficient, the gate length, and modified Plank constant, respectively. Rashba coefficient, $\Delta\alpha$ can be written by $\Delta\alpha = \dfrac{e\hbar^2\Delta E_z}{4m^{*2}c^2} \propto V_G \qquad (4)$

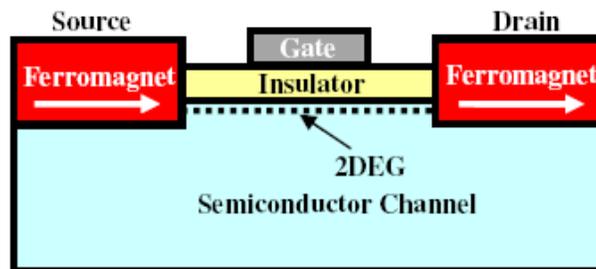where c is light velocity in vacuum.

Figure 2. Configuration of a spin field-effect transistor proposed by Datta and Das. Ferromagnetic source and drain contacts are located on two sides of a semiconductor channel in which spin-polarized current in two dimensional electron gas (2DEG) can be manipulated via gate voltage.

As it can be seen from Figure 2 the basic configuration of proposed device by Datta and Das is almost like today's transistors but it utilizes spin injection and detection properties in its source and drain contacts, respectively. When the magnetization direction of ferromagnetic drain is parallel to that of the majority spin orientation of the electrons at the drain side of the channel, the current can flow through the drain and thus the *on*-state of the spin field-effect transistor is created. By changing the gate voltage the angle of spin precession changes through Rashba effect. Using this property one can induce the preferred alignment to the spins of electrons in semiconductor channel. When the spin alignment between the electrons at the channel end (next to the drain contact) is anti-parallel to the magnetization direction of the drain itself, electrons can not pass through the device any more and the drain current drops sharply because of the magneto resistive nature of this phenomenon. This situation in which the output current is decreased sharply can be interpreted as the *off*-state of the spin field-effect transistor. Changing the gate voltage gives cyclic *on-off* states because of different precession angles which are created with respect to different applied gate voltages.

So far there are two category of controlling spin FET. Spin FET can be controlled by magnetic field (Zeeman effect) and electric field (Rashba effect). Spin state can be separated due to spin-orbit exchange interaction. Spin energy band, Δz in Zeeman effect is given by $\Delta z = g\mu_B B$ 　　　　(5)

where g, μ_B, and B are Zeeman coefficient, magnetic permittance, and magnetic field, respectively. Spin energy band, Δ_R in Rashba effect is written by $\Delta_R = 2\alpha k_F$ 　　　　(6)

where α is Rashba coefficient and given by

$$\alpha = \frac{e\hbar^2 \Delta E_z}{4m^{*2}c^2} = \frac{e\hbar^2}{4m^{*2}c^2 t_{ox}}V_G \qquad (7)$$

Zeeman factors in some semiconductors are big enough and can be listed in table 1.

Table 1. Parameters of semiconductor materials related to Zeeman effect.

Material	E_g [eV] (at 0 K)	Spin-orbital Δ [eV]	Effective mass m^*/m_0	g-factor
GaAs	1.52	0.34	0.067	0.44
Si	1.17	0.044	0.2	2
InAs	0.43	0.43	0.023	15
InSb	0.23	0.32	0.015	51
$Hg_{0.775}Cd_{0.225}Te$	0.12	1.0	0.0075	115

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Rashba factors of some semiconductors used as channel in spin FET are presented in table 2.

We should also note that Rashba factors are too small.

Table 2. Rashba factors of some semiconductors.

Material	α [$\times 10^{-11}$ eV$\times$m]
GaAs	0.04 - 0.08
In$_{0.53}$Ga$_{0.47}$As	0.1 - 0.5
InAs	0.28 – 1.5
InSb	1.16
Hg$_{0.76}$Cd$_{0.24}$Te	3.3

Energy band diagram of spin FET

The basic structure of a spin field-effect transistor is constructed from a metal oxide semiconductor (MOS) gate and two ferromagnetic contacts of source and drain, as it is shown in Figure 2. We also know that the existence of an insulator layer between ferromagnets and semiconductor channel so far has shown a necessity to overcome the problem of conductivity mismatch. Having said that, a variety of band diagrams for different spin field-effect transistors are shown in Figure 3. Ferromagnetic p-n junctions using a ferromagnetic semiconductor and ferromagnetic Schottky junctions using a ferromagnetic metal all can be employed as the source or drain of spin field-effect transistors. Examples of these kinds of junctions are shown in Figure 3 (a) and Figure 3 (b).

Half-metallic ferromagnets are also useful for the ferromagnetic source and drain. The band structure of half-metallic ferromagnets is comprised of metallic and insulating or semiconducting spin bands and thus half-

metallic ferromagnets show one hundred percent spin-polarization at the Fermi energy [7]. The spin-dependent barrier structure appears at the source and drain junctions as it is shown in Figure 3 (c). Another way to realize spin field-effect transistor is to employ tunnel junctions for the ferromagnetic source and drain [8]. So far different kinds of ferromagnetic semiconductors, ferromagnetic metals, and half-metallic ferromagnets have been used for the ferromagnetic electrodes of the tunnel junctions.

When a metallic ferromagnet or a half-metallic ferromagnet is used for the ferromagnetic electrodes of the source or drain, the energy difference between the Fermi energy of the metallic or half-metallic ferromagnet and the conduction band edge of the channel act as an effective Schottky barrier (Φ_{eff}^{SB} shown in Figure 3 (d)). Therefore, control of the effective Schottky barrier height instead of tunnel barrier height or thickness is very essential even for the tunnel junction

contacts in order to tune the junction contact resistance. A spin field-effect transistor can also be comprised of a metal oxide semiconductor gate with a ferromagnetic semiconductor channel and ferromagnetic Schottky junctions for both the source and drain [9].
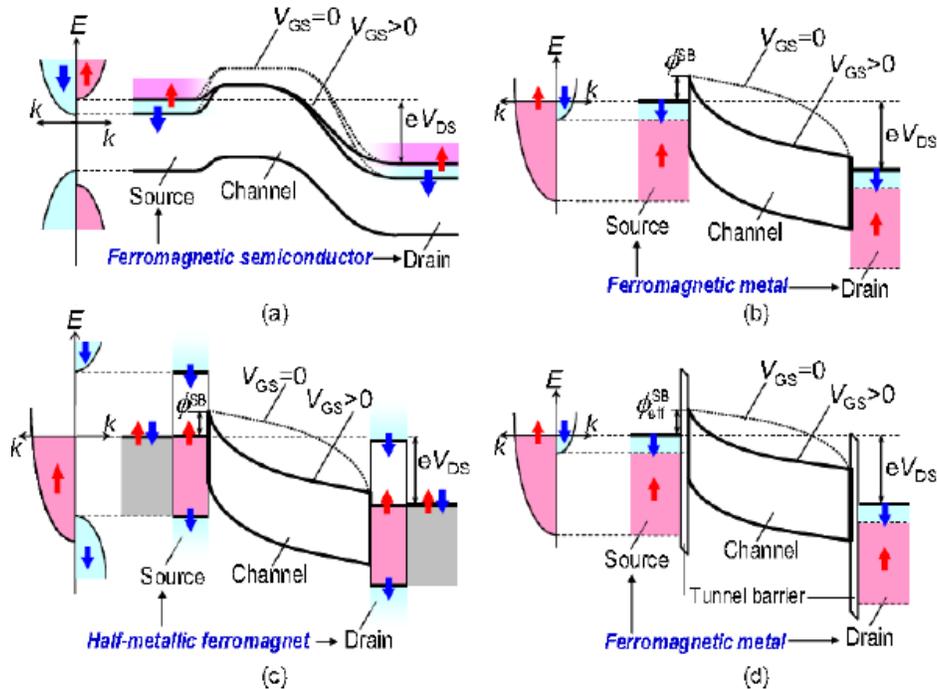

Figure 3. Band diagrams of spin field-effect transistor with: (a) ferromagnetic semiconductor source-drain, (b) ferromagnetic metal source-drain, (c) half-metallic ferromagnet source-drain, and (d) ferromagnetic tunnel contact source-drain [7].

Device structures of spin FET

Ferromagnetic metals are the best candidates for making room temperature spin field-effect transistor source and drain contacts. However, as it was discussed earlier, conductivity mismatch between ferromagnetic metal contacts for source and drain hampers the spin injection into the channel and spin detection in drain. Therefore, spin-dependent interfacial contact resistance (at the source or drain junctions) which is sufficiently larger than the channel resistance is required for efficient spin injection [10]. This increase in interfacial contact resistance decreases the overall device performance as it lowers the total conductance of the transistor device. Since the channel resistance in the *on*-state can be reduced with decreasing the channel length, the spin-dependent contact resistance should also be reduced with decreasing the channel length. Schottky junctions that use very thin low work function interfacial layers are promising

junctions [11] since they can be further down scaled while still maintaining contact resistance character necessary for spin-dependent current injection.

We know that there is a large contact resistance at the source and drain junctions in the ballistic transport regime. This contact resistance deals with the output current and not that of the channel resistance, and hence the conductivity mismatch problem exists even in the ballistic regime [12]. Therefore, spin-dependent contact resistance is required for both diffusive transport and ballistic transport regimes. Since the resistivity of the ferromagnets is comparable to that of the channel, it rules out conductivity mismatch problem [7] and therefore ferromagnetic semiconductors are attractive candidates for source and drain materials. Other possible candidates may are half-metallic ferromagnet contacts with the spin polarization of 100 % [7] for the source and drain contacts.

Two device structures for spin field-effect transistors are shown in Figure 4. We call these structures bulk spin field-effect transistor and silicon on insulator (SOI) spin field-effect transistor corresponding with their configurations. Low production cost for bulk

spin field-effect transistors and excellent device performance for SOI spin field-effect transistors is expected [7]. In the bulk spin field-effect transistor, the ferromagnetic source or drain act as *electrical contacts* to the channel when the transistor is working in its *on*-state, and they work as *blocking contacts* for leakage current between the source and drain when the transistor is in its *off*-state.

We should note that in the bulk spin field-effect transistor; relatively high junction leakage current would be problematic for the Schottky junction contacts. Since the SOI spin field-effect transistor structure considerably minimize the junction area of the source and drain, this device structure is preferable for Schottky junction contacts. The dopant segregation effect during the formation of ferromagnetic silicides and the auto doping effect of epitaxial ferromagnetic metals which are grown on *Si* [13] are also effective to a large extent in reducing the junction leakage current of the ferromagnetic metal source and drain even in the bulk spin field-effect transistor structures.
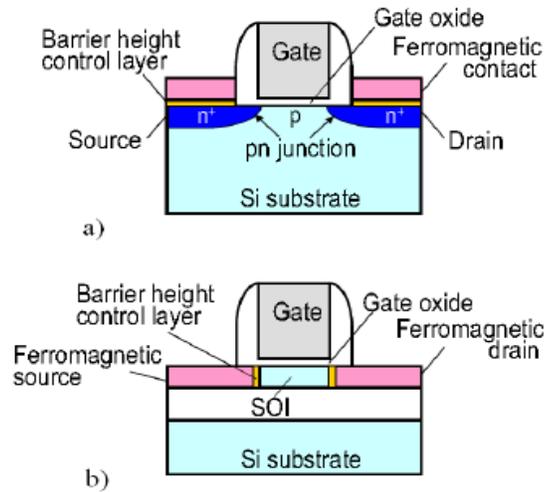
Figure 4. Possible device structures of: (a) bulk spin field-effect transistor and (b) Silicon on insulator (SOI) spin field-effect transistor [7].

One possible device structure of a spin field-effect transistor using nonmagnetic p-n junctions for the source and drain, where ferromagnetic metal or half-metallic ferromagnet contacts are formed on or inside the source and drain regions is shown in Figure 4 (a) (in this figure n$^+$ means highly n-doped). Tunnel contacts due to the Schottky junctions between the ferromagnetic metal and n$^+$ region can be used to remove the conductivity mismatch problem. Since, SiO_2, Si_3N_4, and Al_2O_3 induce only a small density of interface states [7], these materials are promising candidates for interfacial insulating layers. Other prospective materials for the realization of an efficient, high spin injection rate are CoFe/MgO, CoFeB/MgO, and Heusler-alloy/MgO with a low work-function metal layer [7] placed at interfacial barrier to control barrier height.

Another possible device structure of a spin field-effect transistor which uses a thin semiconductor on insulator (SOI) structure is schematically shown in Figure 4 (b). The p-n junction based on ferromagnetic source or drain structures shown in Figure 4 (a) can be also applied to the SOI spin field-effect transistor structure while ferromagnetic Schottky junctions are themselves an alternative candidate. The thin body SOI spin field-effect transistor structure provides several adjustable options in order to improve the device performance.

Typical simulations of spin FET

The flow of current is due to the difference in potentials between the source and the drain, each of which is in a state of local equilibrium, but maintained at different electro-chemical potentials $\mu_{1,2}$ and hence with two distinct Fermi functions:

$$f_1(E) \equiv f_0(E - \mu_1) = \frac{1}{\exp[(E - \mu_1)/k_B T] + 1} \qquad (8)$$

$$f_2(E) \equiv f_0(E - \mu_2) = \frac{1}{\exp[(E - \mu_2)/k_B T] + 1} \qquad (9)$$

by the applied bias V: $\mu_2 - \mu_1 = -qV$. Here, E- energy, k_B - Boltzmann constant, T- temperature.

The density matrix is given by $\rho = \int\limits_{-\infty}^{+\infty} \frac{dE}{2\pi} G^n(E) = \int\limits_{-\infty}^{+\infty} \frac{dE}{2\pi} [A_1(E) f_1(E) + A_2(E) f_2(E)]$ (10)

The current I_D flows in the external circuit is given by Landauer formula:

$$I_D = (q/h) \int\limits_{-\infty}^{+\infty} dE T(E)(f_1(E) - f_2(E)) \quad (11)$$

The quantity T(E) appearing in the current equation (11) is called the transmission function, which tells us the rate at which electrons transmit from the source to the drain contacts by propagating through the device. Knowing the device Hamiltonian [H] and its coupling to the contacts described by the self-energy matrices $\Sigma_{1,2}$, we can calculate the current from (11). For coherent transport, one can calculate the transmission from the Green's function method, using the relation:

$$T(E) = Trace[\Gamma_1 G \Gamma_2 G^+] = Trace[\Gamma_2 G \Gamma_1 G^+] \quad (12)$$

The appropriate NEGF equations are obtained:

$$G = [EI - H - \Sigma_1 - \Sigma_2]^{-1}, \Gamma_{1,2} = i[\Sigma_{1,2} - \Sigma_{1,2}^+], A_1(E) = G\Gamma_1 G^+, A_2(E) = G\Gamma_2 G^+,$$
$$G^n = [A_1]f(E) + [A_2]f(E), A \equiv i[G - G^+] = [A_1] + [A_2] \qquad (13)$$

where H is effective mass Hamiltonian, I is an identity matrix of the same size, $\Gamma_{1,2}$ are the broadening functions, $A_{1,2}$ are partial spectral functions, A(E) are spectral function, G^n is correlation function. We use a discrete lattice with N points spaced by lattice spacing 'a' to calculate the eigenenergies for electrons in the channel.

By utilizing the simulator namely NEMO-VN2 [14], the I_D–V_D characteristics of spin FET having the given parameters are shown in figure 5.

Using "menu" of the main screen we can choose materials, temperature, gate thickness, gate length for simulation of I_D-V_D characteristics of spin FET. Seven semiconductors such as GaAs, Si, InAs, InSb, $Hg_{0.775}Cd_{0.225}Te$ (Table 1) can be chosen for constructing channel of spin FET by using menu. I_D-V_D curves can be divided into two regions: linear and saturation. I_D starts from zero and increases linearly when drain voltage, V_D is small. I_D is not changed when V_D is greater than (V_G – V_{th}), where V_{th} is threshold voltage.
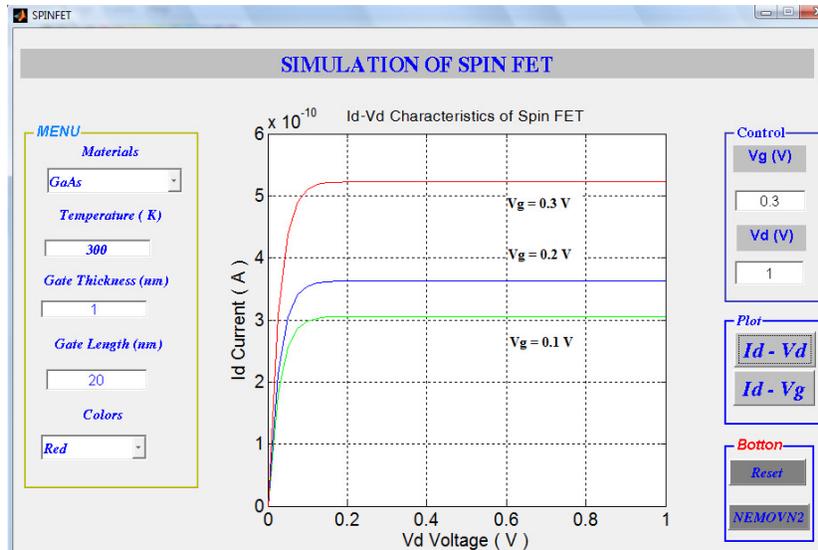
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Figure 5. Typical I_D-V_D characteristics of spin FET simulated by the simulator NEMO-VN2 [14] for various values of V_g = 0.1 V, 0.2 V and 0.3 V at room temperature, T = 300K. The spin FET device parameters are: material, GaAs, L_G = 20 nm, the gate thickness is 1 nm.

Figure 6 demonstrates I_D-V_G characteristics of spin FET at various values of V_D: 0.2 V, 0.3 V; 0.4 V, 0.5 V at room temperature using NEMO-VN2 [14].
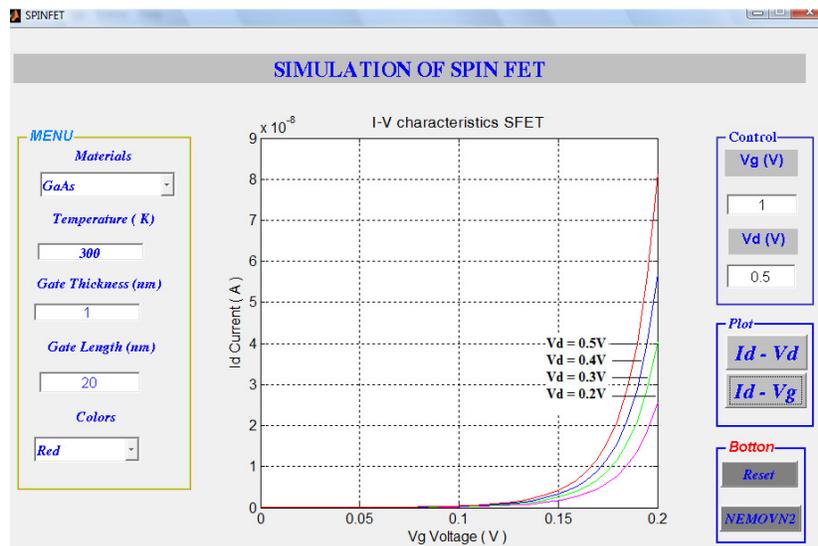

Figure 6. I_D-V_G characteristics simulated by the simulator, NEMO-VN2 [14] at room temperature, T = 300 K for various values of V_D = 0.2V; 0.3V; 0.4V; 0.5V. The parameters of spin FET are: material, GaAs, the gate length, L_G of 20 nm, the gate thickness of 1 nm.

CONCLUSION

A model for spin FET using NEGF written in GUI of Matlab has been reported. The proposed model has been verified by simulating current-voltage characteristics of spin FET. Typical simulations is then successfully performed for various parameters of the spin FET. The model is not only able to accurately describe I_D-V_G, I_D-V_D characteristics of spin FET, but also affects of channel materials, size of spin FET, temperature on characteristics. NEMO-VN2 is a good tool for the development and investigation of quantum device such as spin FET.

MÔ PHỎNG ĐẶC TRƯNG DÒNG-THẾ CỦA SPIN FET SỬ DỤNG NEMO-VN2

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TÓM TẮT: *Chúng tôi đã phát triển bộ mô phỏng cho linh kiện điện tử nano, NEMO-VN2. Trong công trình này, chúng tôi tổng quan về spin FET. Chúng tôi sử dụng bộ mô phỏng này để nghiên cứu kỹ đặc tính của spin FET. Mô hình của spin FET dựa trên phương pháp hàm Green không cân bằng và được hiện thực bằng sử dụng giao diện đồ họa người sử dụng của Matlab. Những đặc trưng dòng-thế như dòng-thế máng, dòng máng - thế cổng được nghiên cứu kỹ.*

Từ khóa: *Transistor spin, spin FET, hàm Green không cân bằng, đặc trưng dòng-thế, đặc trưng dòng-thế máng, đặc trưng dòng máng-thế cổng.*

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