SIMULATION OF CURRENT-VOLTAGE CHARACTERISTICS OF SINGLE ELECTRON TRANSISTOR USING NEMO-VN2

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ABSTRACT: *We have developed a simulator for nanoelectronics devices, NEMO-VN2. In this work we use the simulator to explore the performance of single electron transistor. The model is based on non-equilibrium Green function method and implemented by using graphic user interface of Matlab. The current-voltage characteristics such as drain current-voltage, drain current-gate voltage ones are explored. Some characteristics reproduced by the proposed model are compared with experimental results of single electron transistor and good agreements are validated.*

Keywords: *single electron transistor, non-equilibrium Green function, current-voltage characteristic, Coulomb blockage, Coulomb oscillation.*

INTRODUCTION

Rapid progress in microelectronics has pushed the MOSFET dimension toward the physical limit (10 nm). In the future it is probable that the nanoMOSFETs could be replaced by new fundamental devices, such as single electron transistor (SET). SETs have attracted much attention for IC applications because of their nano feature size, ultra-low power dissipation, high frequency, new functionalities, and CMOS compatible fabrication process. SET shows unique advantages in terms of low power consumption and of new characteristics related to its Coulomb oscillations and Coulomb blockade. Recently, there are various groups achieving success in pursuing to build simulator for SET [1, 2]. The Monte Carlo simulations (e.g. SIMON [3], MOSES [4], and KOSEC [5]) and master equation methods [6, 7] that are quite accurate but also very time consuming, and they are not simple. In contrast, model used non-equilibrium Green function method (NEGF) [8] commonly used in the nanoscale devices and are superior in terms of simplicity.

In this work, we simulate current-voltage characteristics in single electron transistor by non-equilibrium Green function method using graphic user interface (GUI) of Matlab. Here, we use a model of multi level device for SET (i.e. it takes quantumization into account). We also summarize the theoretical approach based on NEGF, review the capabilities of the simulator, NEMO-VN2 [9], give examples of typical simulations of SET's current-voltage characteristics, and compare simulated results with experimental ones.

METHODS

A model of single electron transistor usually called a capacitance model is shown in figure 1. A SET is made from two tunnel junctions that share a common electrode. A tunnel junction consists of two pieces of metal supported by a very thin (about 1 nm) insulator. The only way for electrons is from one of the metal electrodes to travel to the other electrode is to tunnel through the insulator. Since tunneling is a discrete process, the electric charge that flows through the tunnel junction in multiples of e, the charge of electron.

A quantum dot (QD) is usually formed in two dimensional electron gas (2DEG) in GaAs/AlGaAs using standard electron beam lithography. The quantum dot is connected to the source and drain electrodes through tunnel barriers. The potential in the dot can be controlled by the gate electrode which is capacitively coupled to the quantum dot (Figure 1b). The current through the quantum dot can be periodically modulated by the gate voltage (V_G = (2n+1)×e/2C_G, Coulomb oscillations). When the current is zero (Coulomb blockade, CB), the number of electrons is fixed. Therefore it differs exactly by one on both sides of the current peak.

A proper operation of a SET device requires: 1) the tunnel junction resistances (drain resistance, R_D and source resistance, R_S) to be greater than the quantum resistance (25.8 kΩ) to confine the electrons in the quantum dot, 2) the charging energy of the QD capacitance to be larger than the available thermal energy to avoid electron tunneling due to the thermal emission, and the total capacitance is equal to the summation of all device capacitances, i.e. $C_T = C_G + C_D + C_S$.

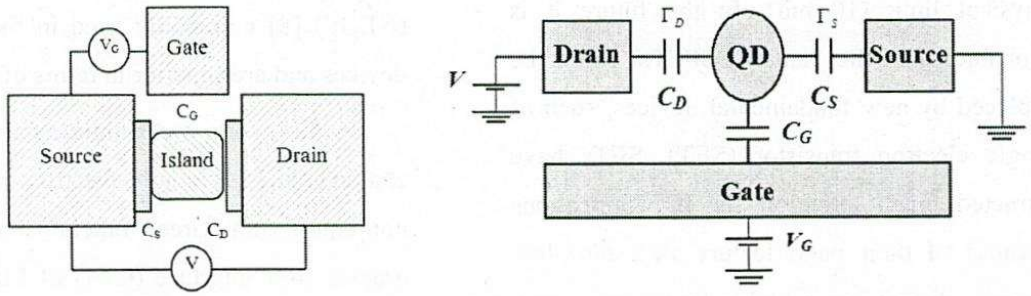


Figure 1. a) Structure of single electron transistor, b) equivalent schematic diagram of SET. The quantum dot is connected to the source and drain electrodes through small tunnel barriers. The potential in the quantum dot can be modified by the gate electrode which is capacitively coupled to the quantum dot ($V_G = (2n+1)e/2C_G$). The DC bias (V_D) is applied and the current is measured as a function of V_D and V_G. The SET's parameters are: C_S, C_D, C_G, Γ_S, Γ_D.

We describe a SET's model for a multi level device whose energy levels are described by a Hamiltonian matrix [H] and whose coupling to the source and the drain contacts is described by self-energy matrices $\left|\sum_1(E)\right|$ and $\left|\sum_2(E)\right|$ respectively (Figure 2).

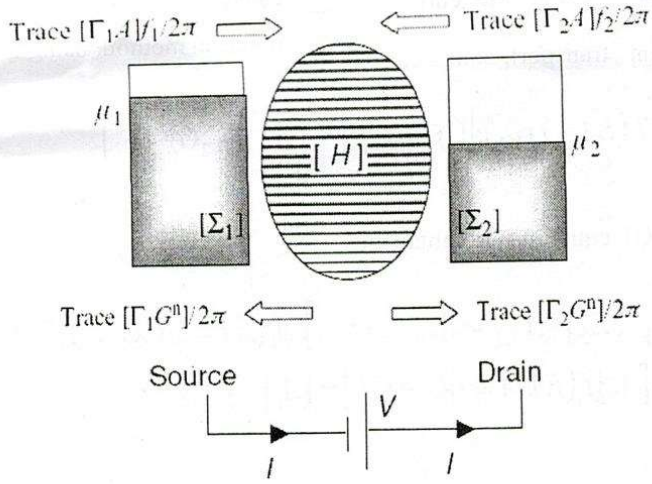


Figure 2. Multi-level device whose energy levels are described by a Hamiltonian matrix [H] and whose coupling to the source and drain contacts is described by self-energy matrices $\left[\sum_1(E)\right]$ and $\left[\sum_2(E)\right]$ respectively.

The flow of current is due to the difference in potentials between the source and the drain, each of which is in a state of local equilibrium, but maintained at different electro-chemical potentials $\mu_{1,2}$ and hence with two distinct Fermi functions:

$$f_1(E) \equiv f_0(E-\mu_1) = \frac{1}{\exp[(E-\mu_1)/k_BT]+1} \quad (1)$$

$$f_2(E) \equiv f_0(E-\mu_2) = \frac{1}{\exp[(E-\mu_2)/k_BT]+1} \quad (2)$$

by the applied bias V: $\mu_2 - \mu_1 = -qV$. Here, E- energy, k_B - Boltzmann constant, T- temperature.

The density matrix is given by

$$\rho = \int_{-\infty}^{+\infty} \frac{dE}{2\pi} G^n(E) = \int_{-\infty}^{+\infty} \frac{dE}{2\pi} [A_1(E) f_1(E) + A_2(E) f_2(E)] \quad (3)$$

The current I_D flows in the external circuit is given by Landauer formula [8]:

$$I_D = (q/h) \int_{-\infty}^{+\infty} dE T(E)(f_1(E) - f_2(E)) \quad (4)$$

The quantity T(E) appearing in the current equation (4) is called the transmission function, which tells us the rate at which electrons transmit from the source to the drain contacts by propagating through the device. Knowing the device Hamiltonian [H] and its coupling to the contacts described by the self-energy

matrices $\Sigma_{1,2}$, we can calculate the current from (4). For coherent transport, one can calculate the transmission from the Green's function method, using the relation

$$T(E) = Trace\left[\Gamma_1 G \Gamma_2 G^+\right] = Trace\left[\Gamma_2 G \Gamma_1 G^+\right] \quad (4)$$

The appropriate NEGF equations are obtained:

$$G = \left[EI - H - \Sigma_1 - \Sigma_2\right]^{-1}, \Gamma_{1,2} = i\left[\Sigma_{1,2} - \Sigma_{1,2}^+\right], A_1(E) = G\Gamma_1 G^+, A_2(E) = G\Gamma_2 G^+, \quad (5)$$
$$G^n = \left[A_1\right] f(E) + \left[A_2\right] f(E), A \equiv i\left[G - G^+\right] = \left[A_1\right] + \left[A_2\right]$$

Where H is effective mass Hamiltonian, I is an identity matrix of the same size, $\Gamma_{1,2}$ are the broadening functions, $A_{1,2}$ are partial spectral functions, A(E) are spectral function, G^n is correlation function. We use a discrete lattice with N points spaced by lattice spacing a to calculate the eigenenergies for electrons in the quantum dot. The Hamiltonian H is given by

$$H = \begin{array}{c|cccccc} & 1 & 2 & \dots & N-1 & N \\ 1 & 2t_0 & -t_0 & & 0 & 0 \\ 2 & -t_0 & 2t_0 & & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ N-1 & 0 & 0 & & 2t_0 & -t_0 \\ N & 0 & 0 & & -t_0 & 2t_0 \end{array} \quad (6)$$

where $t_0 = \dfrac{\hbar^2}{2ma^2}$, m is the effective mass of electron, $\hbar$ is the modified plank constant, a is the lattice spacing in quantum dot.

By utilizing the simulator namely NEMO-VN2, the I_D–V_G characteristics of SET having the given parameters are shown in Figure 3.

RESULTS AND DISCUSSION

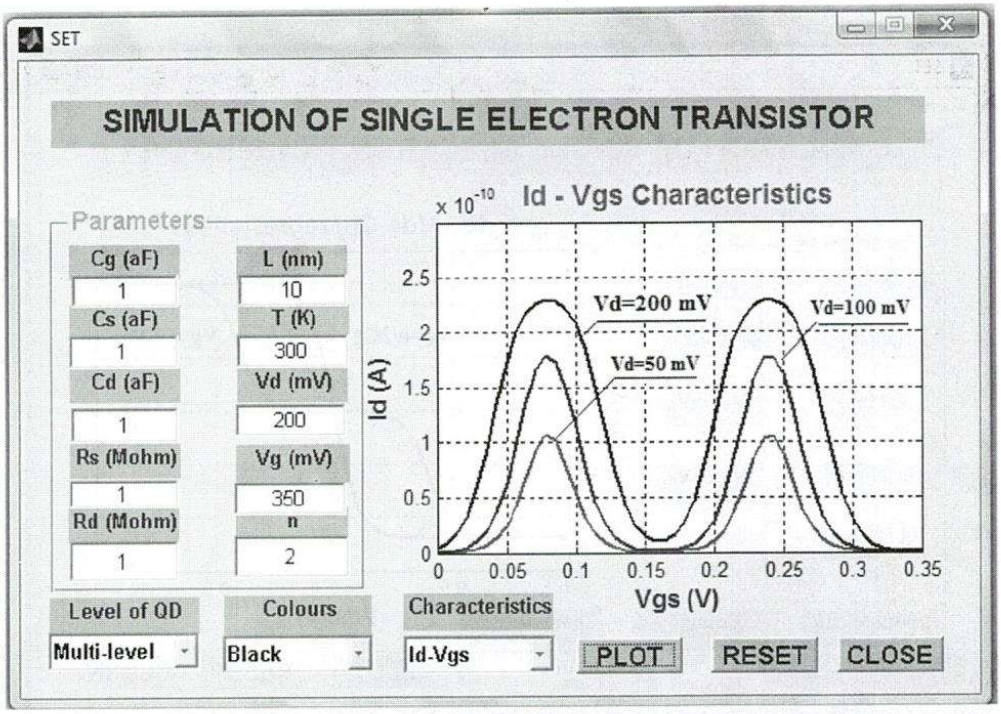


Figure 3. Typical I_D-V_G characteristics (Coulomb oscillations) of SET simulated by the simulator NEMO-VN2 for various values of V_D = 50 mV, 100 mV and 200 mV at room temperature, T = 300K. The SET device parameters are: L = 10 nm, $C_G = C_S = C_D$ = 1aF and $R_S = R_D$ = 1 MΩ .

Figure 3 demonstrates the typical Coulomb oscillation behavior in SET I_D-V_G characteristics. It shows that the SET Coulomb oscillation period (e/C_G, e is the electronic charge) is dictated by SET's gate capacitance. Values of gate voltage at the first and the second peaks are $e/2C_G$ (80 mV) and $3e/2C_G$ (240 mV) respectively. Here, it should be emphasized that the peak and the valley currents of Coulomb oscillations are perfectly represented by the model. The results calculated according to model ($e/2C_G$ for C_G = 1 aF) coincide well with the simulated ones. Current-voltage (I_D-V_G) characteristics showing the suppression of the Coulomb oscillation by broadening current peaks increased at high V_D (200 mV). It also reveals the fact that it is difficult to obtain the Coulomb oscillations in the device characteristics at high V_D greater than $3e/C_T$ (C_T is total capacitance of SET), (160 mV). It should note that high drain voltage, V_D undermines SET's current-voltage characteristics.

Figure 4 reproduces SET's I_D-V_D characteristics at room temperature (T = 300 K) for different gate biases, V_G = 0 mV and $V_G = e/2C_G$ (Coulomb oscillation). For V_G = 0 mV, V_D starts from the Coulomb blockage (CB) region and increases (or decreases) through the single-electron tunneling region. For $V_G = e/2C_G$ (at the first Coulomb oscillation peak), I_D starts from zero and increases (or decreases) linearly.

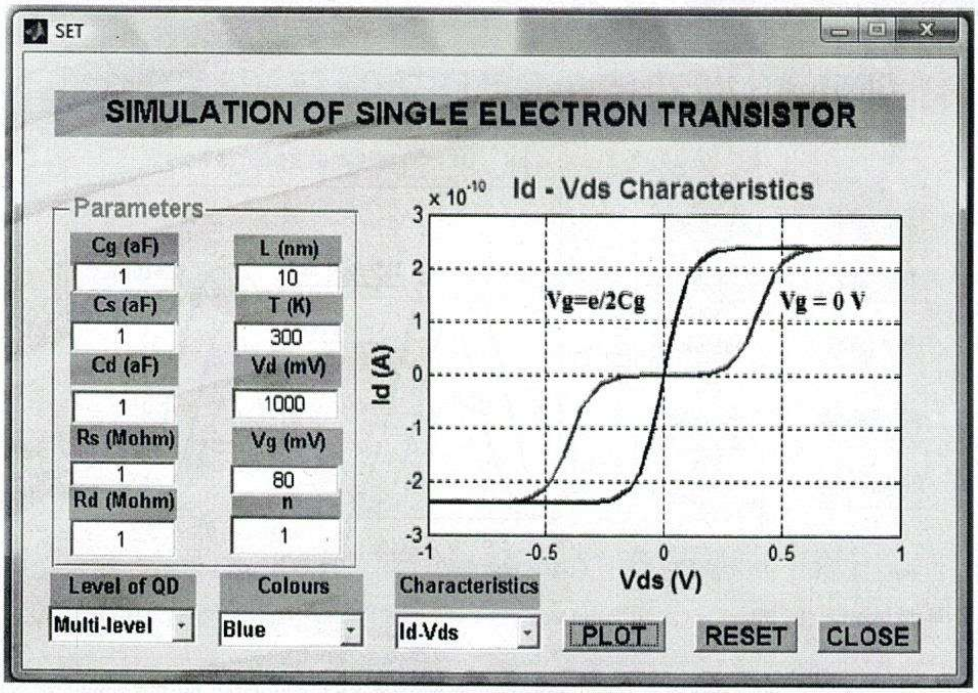


Figure 4. I_D-V_D characteristics simulated by the simulator at room temperature T = 300 K for various values of V_G = 0 mV and V_G = e/2C_G. The SET device parameters are: L = 10 nm, C_G = C_S = C_D = 1 aF and R_S = R_D = 1 MΩ .

Figure 5 represents I_D-V_G characteristics with the value of V_D = 10 mV at different temperatures. One can note that the effects of temperature on Coulomb oscillations are strongly. The Coulomb oscillations of SET are clear at low temperature (at 50 K). Current-voltage (I_D-V_G) characteristics showing the suppression of the Coulomb oscillation by broadening current peaks increased at higher temperature (100 K, 200 K, and 300 K). It also reveals the fact that it is no more possible to obtain the Coulomb oscillations in the device characteristics at high temperature. It should note that high temperature undermines SET's current-voltage characteristics.

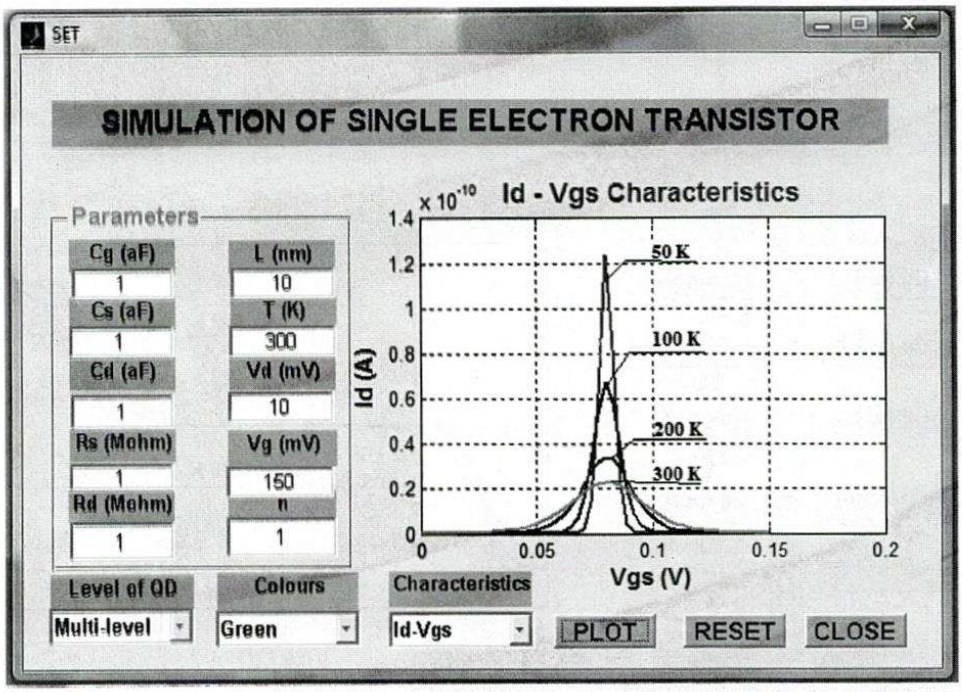


Figure 5. Typical I_D-V_G characteristics simulated by the simulator for value of V_D = 10 mV at different temperatures: 50 K, 100 K, 200 K, 300 K. The SET device parameters are: L = 10 nm, $C_G = C_S = C_D$ = 1aF and $R_S = R_D$ = 1 MΩ

The effect of temperature (T) on the device characteristics is also demonstrated in Figure 6, and it shows that the Coulomb blockade region becomes thinner at higher temperatures. Therefore, an accurate model for SET simulation must be to capture both the effect of temperature and the effect of high V_D on the device characteristics..

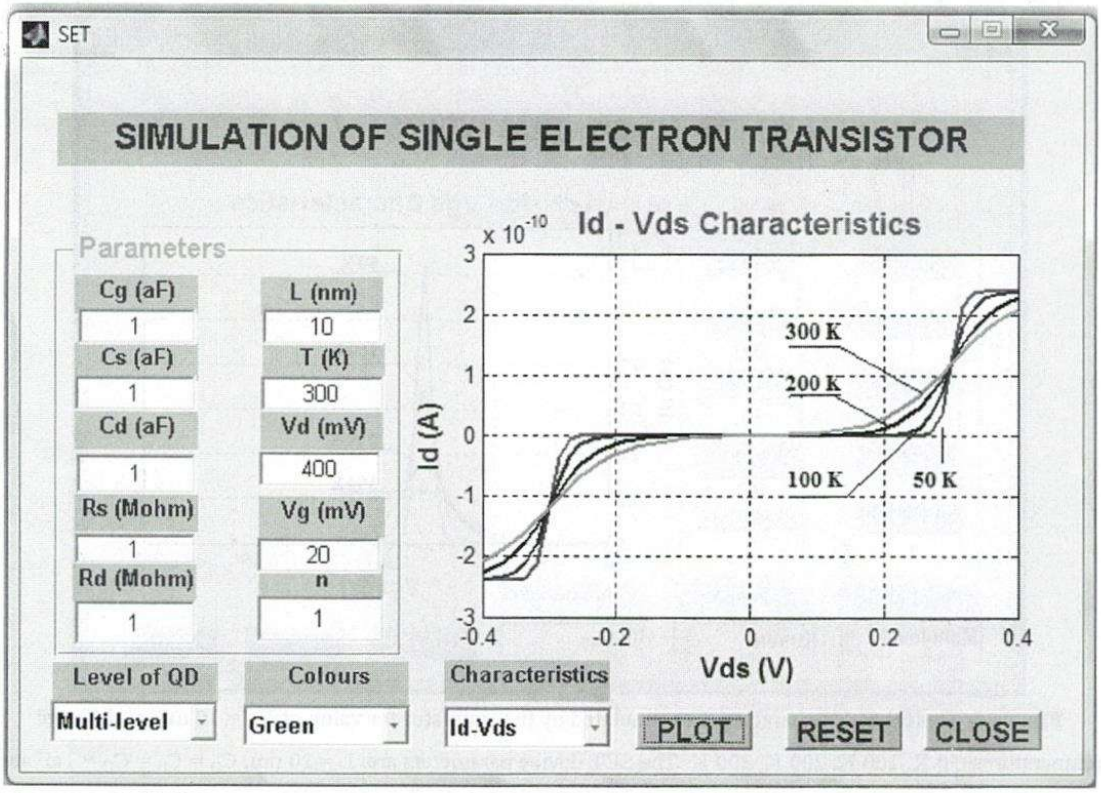
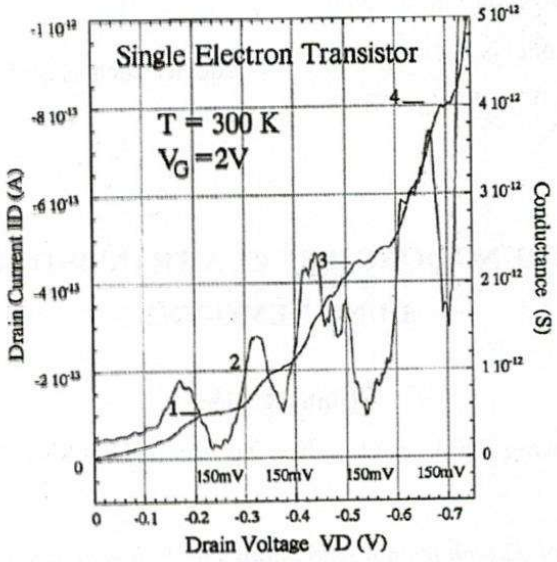


Figure 6. Typical I_D-V_D characteristics simulated by the simulator for value of V_G = 20 mV at different temperatures (T): 50 K, 100 K, 200 K, and 300 K. The SET device parameters are: L = 10 nm, $C_G = C_S = C_D$ = 1aF and $R_S = R_D = 1$ MΩ .

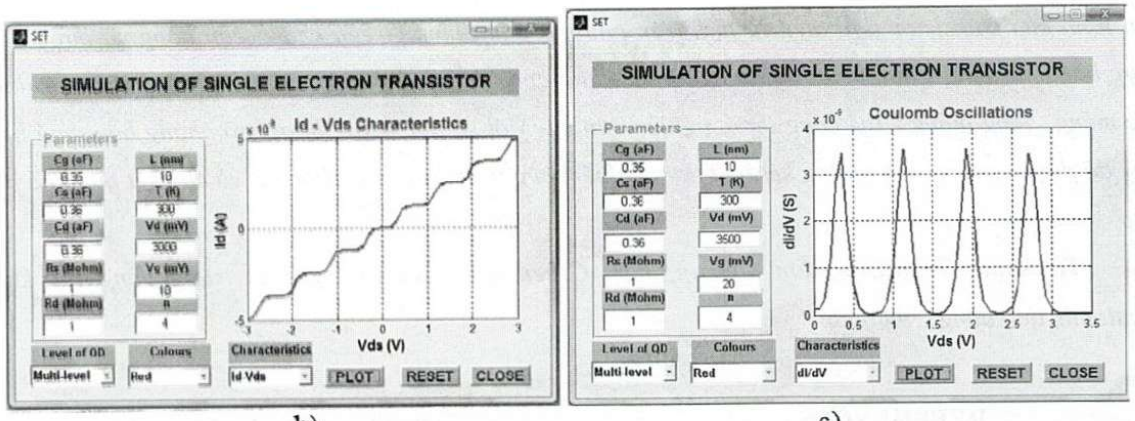
Accuracy of the model is evaluated by comparing simulated results with experimental ones from [10].

According to the work [10], its authors have succeeded in fabricating an SET. The SET operates at room temperature, showing a clear Coulomb staircase with a ~150 mV period at 300 K. The drain current-voltage characteristics of the SET were measured at room temperature and are shown in figure 7a. The gate bias was set to 2 V. In the figure, the solid lines show the current of the SET, and the dashed line shows the conductance of the SET. Between the drain bias of 0 V and -0.75 V, four clear Coulomb staircases with a ~150 mV period are observed. The conductance oscillates with the increase of the drain bias with almost the same 150 mV period. The lower peaks of the conductance oscillation correspond to the flat regions of the current of the Coulomb staircase. The drain current versus gate bias characteristics with 150 mV drain bias at room temperature exhibit clear current oscillations with a period of ~460 mV, implying a periodic Coulomb oscillation of the current. The tunneling capacitance (C_t) and gate capacitance (C_g) could be roughly estimated from the period of the Coulomb staircase and oscillation. Their values were found to be C_t = ~3.6 x 10^{-19} F and C_G = ~3.5 x 10^{-19} F.

Figure 7b,c reproduce I_D-V_D characteristics and conductance of the same SET having length, L = 10 nm at temperature of 300 K. Figures 7b,c show simulated results of I_D-V_D characteristics and conductance of the same SET. Four clear Coulomb staircases are shown in simulated results on I_D-V_D characteristics (Figure 7b). Four clear conductance peaks are also shown in Figure 7c. The results simulated according to the model coincide well with the experimental ones at least in the same shape.



a)



b) c)

Figure 7. a) Drain current versus drain voltage characteristics of the SET at 300 K [10]:V_D = 150 mV, C_t = 0.36 aF, C_G = 0.35 aF ; b) I_D-V_D characteristics simulated; c) Conductance characteristics simulated by the simulator, NEMO-VN2 for value of V_G = 20 mV. The SET device parameters are: L = 10 nm, C_G = 0.35 aF, C_S = C_D = 0.36 aF and R_S = R_D = 1 MΩ .

CONCLUSION

A model for SET device using NEGF written in GUI of Matlab has been reported. The proposed model has been verified at multi level for SET's device. A set of simulations is then successfully performed for various parameters of the SET's device in multi-level mode (i.e. it takes quantumization into account in the quantum dot). The model is not only able to accurately describe I_D-V_G, I_D-V_D SET's characteristics, but also affects of gate materials, size of SET, temperature on SET's characteristics. Different SET's device characteristics (I_D-V_G, I_D-V_D, effect of temperature) have been simulated. The simulated results are also compared with experimental ones [10] and good agreements are validated. NEMO-VN2 is a good tool for the development and investigation of quantum device such as SET.

MÔ PHỎNG ĐẶC TRƯNG DÒNG-THẾ CỦA TRANSISTOR ĐƠN ĐIỆN TỬ SỬ DỤNG NEMO-VN2

Đinh Sỹ Hiền

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TÓM TẮT: *Chúng tôi đã phát triển bộ mô phỏng cho linh kiện điện tử nano, NEMO-VN2. Trong công trình này, chúng tôi sử dụng bộ mô phỏng để nghiên cứu kỹ đặc tính của transistor đơn điện tử. Mô hình của transistor đơn điện tử dựa trên phương pháp hàm Green không cân bằng và được hiện thực bằng sử dụng giao diện đồ họa người sử dụng của Matlab. Những đặc trưng dòng-thế như dòng thế máng, dòng máng - thế cổng được nghiên cứu kỹ. Một số đặc trưng được mô phỏng bằng mô hình này đã được so sánh với những kết quả thực nghiệm của transistor đơn điện tử và cho kết quả khá phù hợp.*

Từ khóa: *Transistor đơn điện tử, hàm Green không cân bằng, đặc trưng dòng-thế, khóa Coulomb, dao động Coulomb.*

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